Verification Methodology For A Complex System On A Chip

CHARME'99 is the tenth in a series of working conferences devoted to the dev- opment and use of leading-edge formal techniques and tools for the design and veri?cation of hardware and systems. Previous conferences have been held in Darmstadt (1984), Edinburgh (1985), Grenoble (1986), Glasgow (1988), Leuven (1989), Torino (1991), Arles (1993), Frankfurt (1995) and Montreal (1997). This workshop and conference series has been organized in cooperation with IFIP WG 10. 5. It is now the biannual counterpart of FMCAD, which takes place every even-numbered year in the USA. The 1999 event took place in Bad Her- nalb, a resort village located in the Black Forest close to the city of Karlsruhe. The validation of functional and timing behavior is a major bottleneck in current VLSI design systems. A predominantly academic area of study until a few years ago, formal design and veri?cation techniques are now migrating into industrial use. The aim of CHARME'99 is to bring together researchers and users from academia and industry working in this active area of research. Two invited talks illustrate major current trends: the presentation by G ?erard Berry (Ecole des Mines de Paris, Sophia-Antipolis, France) is concerned with the use of synchronous languages in circuit design, and the talk given by Peter Jansen (BMW, Munich, Germany) demonstrates an application of formal methods in an industrial environment. The program also includes 20 regular presentations and 12 short presentations/poster exhibitions that have been selected from the 48 submitted papers.

The biannual Formal Methods in Computer Aided Design conference (FMCAD 2000)is the third in a series of conferences under that title devoted to the use of discrete mathematical methods for the analysis of computer hardware and so- ware. The work reported in this book describes the use of modeling languages and their associated automated analysis tools to specify and verify computing systems. Functional veric ation has become one of the principal costs in a modern computer design e ort. In addition,verica tion of circuit models, timing,power, etc., requires even more eo rt. FMCAD provides a venue for academic and - dustrial researchers and practitioners to share their ideas and experiences of using discrete mathematical modeling and veric ation. It is noted with interest by the conference chairmen how this area has grown from just a few people 15 years ago to a vibrant area of research, development, and deployment. It is clear that these methods are helping reduce the cost of designing computing systems. As an example of this potential cost reduction, we have invited David Russino of Advanced Micro Devices, Inc. to describe his veric ation of ?oating-point - gorithms being used in AMD microprocessors. The program includes 30 regular presentations selected from 63 submitted papers.

This book constitutes the proceedings of the 14th International Conference on Applied Reconfigurable Computing, ARC 2018, held in Santorini, Greece, in May 2018. The 29 full papers and 22 short presented in this volume were carefully reviewed and selected from 78 submissions. In addition, the volume contains 9 contributions from research projects. The papers were organized in topical sections named: machine learning and neural networks; FPGA-based design and CGRA optimizations; applications and surveys; fault-tolerance, security and communication architectures; reconfigurable and adaptive architectures; design methods and fast prototyping; FPGA-based design and applications; and special session: research projects.

The creation of a computer system has become a monumental task. Many designers, engineers, and scientists cooperate to create the computer system down to its most basic components. An extremely crucial phase of the design of the hardware sub-systems is the verification of the hardware paradigms and structures that will work in synch to create the new computer system. Therefore, the verification of a system level chip is quite a complex task. Moreover, the verification process in any design is considered a major bottleneck, but it is required to ensure that the number of errors in the hardware designs is minimized. It can be safely said that the complexity of verification increases exponentially with the increase in design complexity [1]. This thesis demonstrates the application of the two level verification methodologies to the inter-processor communication module of the Cyclops 64 architecture. (Abstract shortened by UMI.).

Annual Report

Design and Verification Methodology for Complex Three-Dimensional Digital Integrated Circuit

Applied Reconfigurable Computing. Architectures, Tools, and Applications

Advances in Computing Systems and Applications

A SystemC Based Approach for Successful Tapeout

5th International Conference, FMCAD 2004, Austin, Texas, USA, November 15-17, 2004, Proceedings

10th IFIP WG10.5 Advanced Research Working Conference, CHARME'99, Bad Herrenalb, Germany, September 27-29, 1999, Proceedings

Verification is increasingly complex, and SystemVerilog is one of the languages that the verification community is turning to. However, no language by itself can guarantee success without proper techniques. Object-oriented programming (OOP), with its focus on managing complexity, is ideally suited to this task. With this handbook—the first to focus on applying OOP to SystemVerilog—we'll show how to manage complexity by using layers of abstraction and base classes. By adapting these techniques, you will write more "reasonable" code, and build efficient and reusable verification components. Both a learning tool and a reference, this handbook contains hundreds of real-world code snippets and three professional verification-system examples. You can copy and paste from these examples, which are all based on an open-source, vendor-neutral framework (with code freely available at www.trusster.com). Learn about OOP techniques such as these: Creating classes—code interfaces, factory functions, reuse Connecting classes—pointers, inheritance, channels Using "correct by construction"—strong typing, base classes Packaging it up—singletons, static methods, packages

Engineering the Complex SOC The first unified hardware/software guide to processor-centric SOC design Processor-centric approaches enable SOC designers to complete far larger projects in far less time. Engineering the Complex SOCis a comprehensive, example-driven guide to creating designs with configurable, extensible processors. Drawing upon Tensilica's Xtensa architecture and TIE language, Dr. Chris Rowen systematically illuminates the issues, opportunities, and challenges of processor-centric design. Rowen introduces a radically new design methodology, then covers its essential techniques: processor configuration, extension, hardware/software co-generation, multiple processor partitioning/communication, and more. Coverage includes: Why extensible processors are necessary: shortcomings of current design methods Comparing extensible processors to traditional processors and hardwired logic Extensible processor architecture and mechanisms of processor extensibility Latency, throughput, coordination of parallel functions, hardware interconnect options, management of design complexity, and other issues Multiple-processor SOC architecture for embedded systems Task design from the viewpoints of software andhardware developers Advanced techniques: implementing complex state machines, task-to-task synchronization, power optimization, and more Toward a "sea of processors": Long-term trends in SOC design and semiconductor technology For all architects, hardware engineers, software designers, and SOC program managers involved with complex SOC design; and for all managers investing in SOC designs, platforms, processors, or expertise. PRENTICE HALL Professional Technical Reference Upper Saddle River, NJ 07458 www.phptr.com

System-On-a-Chip Verification: Methodology and Techniques is the first book to cover verification strategies and methodologies for SOC verification from system level verification to the design sign- off. The topics covered include Introduction to the SOC design and verification aspects, System level verification in brief, Block level verification, Analog/mixed signal simulation, Simulation, HW/SW Co-verification, Static netlist verification, Physical verification, and Design sign-off in brief. All the verification aspects are illustrated with a single reference design for Bluetooth application. System-On-a-Chip Verification: Methodology and Techniques takes a systematic approach that covers the following aspects of verification strategy in each chapter: Explanation of the objective involved in performing verification after a given design step; Features of options available; When to use a particular option; How to select an option; and Limitations of the option. This exciting new book will be of interest to all designers and test professionals.

The Automated Technology for Veri?cation and Analysis (ATVA) international symposium series was initiated in 2003, responding to a growing interest in formal veri?cation spurred by the booming IT industry, particularly hardware design and manufacturing in East Asia. Its purpose is to promote research on automated veri?cation and analysis in the region by providing a forum for int- action between the regional and the international research/industrial commu- ties of the ?eld. ATVA 2005, the third of the ATVA series, was held in Taipei, Taiwan, October 4-7, 2005. The main theme of the symposium encompasses - sign, complexities, tools, and applications of automated methods for veri?cation and analysis. The symposium was co-located and had a two-day overlap with FORTE 2005, which was held October 2-5, 2005. We received a total of 95 submissions from 17 countries. Each submission was assigned to three Program Committee members, who were helped by their subreviewers, for rigorous and fair evaluation. The ?nal deliberation by the P- gram Committee was conducted over email for a duration of about 10 days after nearly all review reports had been collected. In the end, 33 papers were - lectedforinclusionintheprogram.ATVA2005hadthreekeynotespeechesgiven respectively by Amir Pnueli (joint with FORTE 2005), Zohar Manna, and Wo- gang Thomas. The main symposium was preceded by a tutorial day, consisting of three two-hour lectures given also by the keynote speakers.

34th IFIP WG 6.1 International Conference, FORTE 2014, Held as Part of the 9th International Federated Conference on Distributed Computing Techniques, DisCoTec 2014, Berlin, Germany, June 3-5, 2014, Proceedings

Correct Hardware Design and Verification Methods

Engineering the Complex SOC

Software Technologies

TLM-driven Design and Verification Methodology

15th International Conference, ICSOFT 2020, Online Event, July 7-9, 2020, Revised Selected Papers

Open Verification Methodology Cookbook

A Hierarchical Analysis and Verification Methodology for Complex VLSI Systems [microform]National Library of CanadaDesign and Verification Methodology for Complex Three-dimensional Digital Integrated Circuit

This book constitutes the refereed proceedings of the 20th International Symposium on Formal Methods, FM 2015, held in Oslo, Norway, in June 2015. The 30 full papers and 2 short papers presented were carefully reviewed and selected from 124 submissions. The papers cover a wide spectrum of all the different aspects of the use of and the research on formal methods for software development.

This book describes a comprehensive SystemC TLM-driven IP design and verification solution'including methodology guidelines, high-level synthesis, and TLM-aware verification basedon Cadence products'that will help designers transition to a TLM-driven design andverification flow.

These are the proceedings of the fifth international conference, Formal Methods in Computer-Aided Design (FMCAD), held 15-17 November 2004 in Austin, Texas, USA. The conference provides a forum for presenting state-of-the-art tools, methods, algorithms, and theory for the application of formalized reasoning to all aspects of computer-aided system design, including specification, verification, synthesis, and testing. FMCAD's heritage dates back 20 years to some of the earliest conferences on the subject of formal reasoning and computer-aided design. Since 1996,FMCAD has assumed its present form, held biennially in North America, alternating with its sister conference CHARME in Europe. We are delighted to report that our research community continues to flourish: we received 69 paper submissions, with many more high-quality papers than we had room to accept. After a rigorous review process, in which each paper received at least three, and typically four or more, independent reviews, we accepted 29 papers for the conference and inclusion in this volume. The conference also included invited talks from Greg Spirakis of Intel Corporation and Wayne Wolf of Princeton University. A conference of this size requires the contributions of numerous people. On the technical side, we are grateful to the program committee and the additional reviewers for their countless hours reviewing submissions and ensuring the intellectual quality of the conference. We would also like to thank the steering committee for their wisdom and guidance. On the logistical side, we thank Christa Mace for designing our website and attending to countless organizational tasks. And we thank our corporate sponsors - AMD, IBM, Intel, and Synopsys - for financial support that helped make this conference possible.

Third International Symposium, ATVA 2005, Taipei, Taiwan, October 4-7, 2005, Proceedings

System-level Test and Validation of Hardware/Software Systems

Third International Conference, FMCAD 2000 Austin, TX, USA, November 1-3, 2000 Proceedings

PROCEEDINGS OF THE 20TH CONFERENCE ON FORMAL METHODS IN COMPUTER-AIDED DESIGN – FMCAD 2020

14th International Symposium, ARC 2018, Santorini, Greece, May 2-4, 2018, Proceedings

Comprehensive Functional Verification

First International Conference, FMCAD '96, Palo Alto, CA, USA, November 6 - 8, 1996, Proceedings

Professional Verification is a guide to advanced functional verification in the nanometer era. It presents the best practices in functional verification used today and provides insights on how to solve the problems that verification teams face. Professional Verification is based on the experiences of advanced verification teams throughout the industry, along with work done at Cadence Design Systems. Professional Verification presents a complete and detailed Unified Verification Methodology based on the best practices in use today. It also addresses topics important to those doing advanced functional verification, such as assertions, functional coverage, formal verification, and reactive testbenches.

The Accellera Universal Verification Methodology (UVM) standard is architected to scale, but verification is growing and in more than just the digital design dimension. It is growing in the SoC dimension to include low-power and mixed-signal and the system integration dimension to include multi-language support and acceleration. These items and others all contribute to the quality of the SOC so the Metric-Driven Verification (MDV) methodology is needed to unify it all into a coherent verification plan. This book is for verification engineers and managers familiar with the UVM and the benefits it brings to digital verification but who also need to tackle specialized tasks. It is also written for the SoC project manager that is tasked with building an efficient worldwide team. While the task continues to become more complex, Advanced Verification Topics describes methodologies outside of the Accellera UVM standard, but that build on it, to provide a way for SoC teams to stay productive and profitable.

One of the biggest challenges in chip and system design is determining whether the hardware works correctly. That is the job of functional verification engineers and they are the audience for this comprehensive text from three top industry professionals. As designs increase in complexity, so has the value of verification engineers within the hardware design team. In fact, the need for skilled verification engineers has grown dramatically--functional verification now consumes between 40 and 70% of a project's labor, and about half its cost. Currently there are very few books on verification for engineers, and none that cover the subject as comprehensively as this text. A key strength of this book is that it describes the entire verification cycle and details each stage. The organization of the book follows the cycle, demonstrating how functional verification engages all aspects of the overall design effort and how individual cycle stages relate to the larger design process. Throughout the text, the authors leverage their 35 plus years experience in functional verification, providing examples and case studies, and focusing on the skills, methods, and tools needed to complete each verification task. Comprehensive overview of the complete verification cycle Combines industry experience with a strong emphasis on functional verification fundamentals Includes real-world case studies

This book constitutes the refereed proceedings of the First International Conference on Formal Methods in Computer-Aided Design, FMCAD '96, held in Palo Alto, California, USA, in November 1996. The 25 revised full papers presented were selected from a total of 65 submissions; also included are three invited survey papers and four tutorial contributions. The volume covers all relevant formal aspects of work in computer-aided systems design, including verification, synthesis, and testing.

Automated Technology for Verification and Analysis

Mixed-Signal Methodology Guide

High-Level Modeling and Directed Test Generation Techniques

Tower Methodology for Verification of Multi-core Architecture

Formal Techniques for Distributed Objects, Components, and Systems

SystemVerilog for Verification

Proceedings of the 4th Conference on Computing Systems and Applications

This proceedings book gathers selected papers presented at the 4th Conference on Computing Systems and Applications (CSA2020) held on December 14, 2020, at the Ecole Militaire Polytechnique, Algiers, Algeria. The proceedings provide a collection of new ideas, original research findings, and experimental results in the field of computer science covering: artificial intelligence, data science, computer networks and security, information systems, software engineering, and computer graphics. The proceedings are a valuable reference work for students, researchers, academics, and industry practitioners interested in the latest scientific and technological advances across the conference topics. Benefits: " Explores the latest research trends and their applications in a broad range of computer science disciplines " Presents a collection of contributions in emerging topics in computer science and information technology " Covers artificial intelligence, data science, computer networks and security, information systems, software engineering, and computer graphics.

From past decades, Computational intelligence embraces a number of nature-inspired computational techniques which mainly encompasses fuzzy sets, genetic algorithms, artificial neural networks and hybrid neuro-fuzzy systems to address the computational complexities such as uncertainties, vagueness and stochastic nature of various computational problems practically. At the same time, Intelligent Control systems are emerging as an innovative methodology which is inspired by various computational intelligence process to promote a control over the systems without the use of any mathematical models. To address the effective use of intelligent control in Computational intelligence systems, International Conference on Intelligent Computing, Information and Control Systems (ICICCS 2019) is initiated to encompass the various research works that helps to develop and advance the next-generation intelligent computing and control systems. This book integrates the computational intelligence and intelligent control systems to provide a powerful methodology for a wide range of data analytics issues in industries and societal applications. The recent research advances in computational intelligence and control systems are addressed, which provide very promising results in various industry, business and societal studies. This book also presents the new algorithms and methodologies for promoting advances in common intelligent computing and control methodologies including evolutionary computation, artificial life, virtual infrastructures, fuzzy logic, artificial immune systems, neural networks and various neuro-hybrid methodologies. This book will be pragmatic for researchers, academicians and students dealing with mathematically intransigent problems. It is intended for both academicians and researchers in the field of Intelligent Computing, Information and Control Systems, along with the distinctive readers in the fields of computational and artificial intelligence to gain more knowledge on Intelligent computing and control systems and their real-world applications.

Formal Methods in Computer-Aided Design (FMCAD) is a conference series on the theory and applications of formal methods in hardware and system verification. FMCAD provides a leading forum to researchers in academia and industry for presenting and discussing ground-breaking methods, technologies, theoretical results, and tools for reasoning formally about computing systems. FMCAD covers formal aspects of computer-aided system design including verification, specification, synthesis, and testing.

This four-volume set (CCIS 643, 644, 645, 646) constitutes the refereed proceedings of the 16th Asia Simulation Conference and the First Autumn Simulation Multi-Conference, AsiaSim / SCS AutumnSim 2016, held in Beijing, China, in October 2016. The 265 revised full papers presented were carefully reviewed and selected from 651 submissions. The papers in this first volume of the set are organized in topical sections on modeling and simulation theory and methodology; model engineering for system of systems; high performance computing and simulation; modeling and simulation for smart city.

Verification Methodology Manual for SystemVerilog

IFIP TC10 WG10.5 Tenth International Conference on Very Large Scale Integration (VLSI ' 99) December 1 – 4, 1999, Lisboa, Portugal

FM 2015: Formal Methods

A Practical Guide to Adopting the Universal Verification Methodology (UVM) Second Edition

A Guide to Advanced Functional Verification

Automated Low-Altitude Air Delivery

Theory, Methodology, Tools and Applications for Modeling and Simulation of Complex Systems

This book provides practical information for hardware and software engineers using the SystemVerilog language to verify electronic designs. The authors explain methodology concepts for constructing testbenches that are modular and reusable. The text includes extensive coverage of the SystemVerilog 3.1a constructs, and reviews SystemVerilog 3.0 topics such as interfaces and data types. Included are detailed explanations of Object Oriented Programming and information on testbenches, multithreaded code, and interfacing to hardware designs.

Offers users the first resource guide that combines both the methodology and basics of SystemVerilog Addresses how all these pieces fit together and how they should be used to verify complex chips rapidly and thoroughly. Unique in its broad coverage of SystemVerilog, advanced functional verification, and the combination of the two.

This book constitutes the refereed proceedings of the 11th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods, CHARME 2001, held in Livingston, Scotland, UK in September 2001. The 28 revised full papers and eight short papers presented together with two invited papers and one special paper were carefully reviewed and selected from 56 submissions. The book offers topical sections on model checking, clocking issues, theorem proving with higher order logics, hardware compilation, tools, component verification, case studies, algorithm verification, and duration calculus.

Three-Dimensional Integrated Circuits (3DICs) have recently attracted great interest from researchers and IC designers as a possible solution to fill the gap between device and interconnect scaling. Various studies have demonstrated the potential performance improvement of 3DICs by eliminating long interconnects, repeaters, and clock buffers.

Formal Methods in Computer-Aided Design

Towards Autonomous Cargo Transportation with Drones

Assessing the Reliability of Complex Models

Methodology and Techniques

VLSI: Systems on a Chip

Applications in Electronics Pervading Industry, Environment and Society

The Complete Industry Cycle

This book covers state-of-the art techniques for high-level modeling and validation of complex hardware/software systems, including those with multicore architectures. Readers will learn to avoid time-consuming and error-prone validation from the comprehensive coverage of system-level validation, including high-level modeling of designs and faults, automated generation of directed tests, and efficient validation methodology using directed tests and assertions. The methodologies described in this book will help designers to improve the quality of their validation, performing as much validation as possible in the early stages of the design, while reducing the overall validation effort and cost.

This book provides a thorough overview of cutting-edge research on electronics applications relevant to industry, the environment, and society at large. It covers a broad spectrum of application domains, from automotive to space and from health to security, while devoting special attention to the use of embedded devices and sensors for imaging, communication and control. The book is based on the 2015 ApplePies Conference, held in Rome, which brought together researchers and stakeholders to consider the most significant current trends in the field of applied electronics and to debate visions for the future. Areas addressed by the conference included information communication technology; biotechnology and biomedical imaging; space; secure, clean and efficient energy; the environment; and smart, green and integrated transport. As electronics technology continues to develop apace, constantly meeting previously unthinkable targets, further attention needs to be directed toward the electronics applications and the development of systems that facilitate human activities. This book, written by industrial and academic professionals, represents a valuable contribution in this endeavor.

This book constitutes the thoroughly refereed proceedings of the 15th International Conference on Software Technologies, ICSOFT 2020, which was held virtually due to the Covid-19 pandemic. The 12 revised full papers were carefully reviewed and selected from 95 submissions. The papers deal with the following topics: business process modelling; IT service management; interoperability and service-oriented architecture; project management software; scheduling and estimating; software metrics; requirements elicitation and specification; software and systems integration among others.

New manufacturing technologies have made possible the integration of entire systems on a single chip. This new design paradigm, termed system-on-chip (SOC), together with its associated manufacturing problems, represents a real challenge for designers. SOC is also reshaping approaches to test and validation activities. These are beginning to migrate from the traditional register-transfer or gate levels of abstraction to the system level. Until now, test and validation have not been supported by system-level design tools so designers have lacked the infrastructure to exploit all the benefits stemming from the adoption of the system level of abstraction. Research efforts are already addressing this issue. This monograph provides a state-of-the-art overview of the current validation and test techniques by covering all aspects of the subject including: modeling of bugs and defects; stimulus generation for validation and test purposes (including timing errors; design for testability.

System-Level Validation

Mathematical and Statistical Foundations of Verification, Validation, and Uncertainty Quantification

Advanced Verification Techniques

A Hierarchical Analysis and Verification Methodology for Complex VLSI Systems [microform]

Advanced Verification Topics

An Object-Oriented Framework

The past fifty years have seen rapid development of public and governmental awareness of environmental issues. Engineers and scientists have made tangible contributions to environmental protection. However, further theoretical and practical developments are necessary to address mankinds growing demands on the environment. Construction for a Sustai

Three-Dimensional Integrated Circuits (3DICs) have recently attracted great interest from researchers and IC designers as a possible solution to fill the gap between device and interconnect scaling. Various studies have demonstrated the potential performance improvement of 3DICs by eliminating long interconnects, repeaters, and clock buffers. Though 3DICs are attractive, there are significant challenges associated with this topic. The most fundamental issue in 3DIC is heat dissipation. The thermal effect has impacted the conventional high-performance 2DICs in deep sub-micron technology nodes. Its effect will aggravate 3DICs due to two major reasons: higher power density, and lower thermal conductivity caused by more insulating dielectric layers. Furthermore, while 3D integration provides more design flexibility, this technology also introduces much higher design complexity. The existing 2D physical design methodology cannot be simply extended to a 3D case because of the huge obstacles in the z-direction and thermal constraints. Efficient design flows and algorithms must be developed to facilitate 3DIC design. This dissertation proposes a design and verification methodology, along with analyses of delay, thermal, and reliability of a 3D system. The methodology uses commercial 2D CAD tools with Python and Tcl scripts to link them together. The scripts modify the output files (or databases) of the commercial tools and add 3D features to them. The entire flow achieves RTL-to-GDSII physical design automation for 3DICs. Design trade-offs and timing reliability of 3D systems are two other major issues of this dissertation. Non-idealities threaten to diminish the benefit and may cause reliability problems in 3D systems. These non-idealities must be monitored during the design procedure. With a fast yet accurate temperature dependency model, these non-idealities were successfully taken into consideration during both design and verification phases. The final performance analy.

"As chip size and complexity continues to grow exponentially, the challenges of functional verification are becoming a critical issue in the electronics industry. It is now commonly heard that logical errors missed during functional verification are the most common cause of chip re-spins, and that the costs associated with functional verification are now outweighing the costs of chip design. To cope with these challenges engineers are increasingly relying on new design and verification methodologies and languages. Transaction-based design and verification, constrained random stimulus generation, functional coverage analysis, and assertion-based verification are all techniques that advanced design and verification teams routinely use today. Engineers are also increasingly turning to design and verification models based on C/C++ and SystemC in order to build more abstract, higher performance hardware and software models and to escape the limitations of RTL HDLs. This new book, Advanced Verification Techniques, provides specific guidance for these advanced verification techniques. The book includes realistic examples and shows how SystemC and SCV can be applied to a variety of advanced design and verification tasks." - Stuart Swan

Functional verification is an art as much as a science. It requires not only creativity and cunning, but also a clear methodology to approach the problem. The Open Verification Methodology (OVM) is a leading-edge methodology for verifying designs at multiple levels of abstraction. It brings together ideas from electrical, systems, and software engineering to provide a complete methodology for verifying large scale System-on-Chip (SoC) designs. OVM defines an approach for developing testbench architectures so they are modular, configurable, and reusable. This book is designed to help both novice and experienced verification engineers master the OVM through extensive examples. It describes basic verification principles and explains the essentials of transaction-level modeling (TLM). It leads readers from a simple connection of a producer and a consumer through complete self-checking testbenches. It explains construction techniques for building configurable, reusable testbench components and how to use TLM to communicate between them. Elements such as agents and sequences are explained in detail.

Construction for a Sustainable Environment

A Case Study

Fast, Flexible Design with Configurable Processors

20th International Symposium, Oslo, Norway, June 24-26, 2015, Proceedings

16th Asia Simulation Conference and SCS Autumn Simulation Multi-Conference, AsiaSim/SCS AutumnSim 2016, Beijing, China, October 8-11, 2016, Proceedings, Part I

A Guide to Learning the Testbench Language Features

ICICCS 2019

Advances in computing hardware and algorithms have dramatically improved the ability to simulate complex processes computationally. Today's simulation capabilities offer the prospect of addressing questions that in the past could be addressed only by resource-intensive experimentation, if at all. Assessing the Reliability of Complex Models recognizes the ubiquity of uncertainty in computational estimates of reality and the necessity for its quantification. As computational science and engineering have matured, the process of quantifying or bounding uncertainties in a computational estimate of a physical quality of interest has evolved into a small set of interdependent tasks: verification, validation, and uncertainty of quantification (VVUQ). In recognition of the increasing importance of computational simulation and the increasing need to assess uncertainties in computational results, the National Research Council was asked to study the mathematical foundations of VVUQ and to recommend steps that will ultimately lead to improved processes. Assessing the Reliability of Complex Models discusses changes in education of professionals and dissemination of information that should enhance the ability of future VVUQ practitioners to improve and properly apply VVUQ methodologies to difficult problems, enhance the ability of VVUQ customers to understand VVUQ results and use them to make informed decisions, and enhance the ability of all VVUQ stakeholders to communicate with each other. This report is an essential resource for all decision and policy makers in the field, students, stakeholders, UQ experts, and VVUQ educators and practitioners.

For over three decades now, silicon capacity has steadily been doubling every year and a half with equally staggering improvements continuously being observed in operating speeds. This increase in capacity has allowed for more complex systems to be built on a single silicon chip. Coupled with this functionality increase, speed improvements have fueled tremendous advancements in computing and have enabled new multi-media applications. Such trends, aimed at integrating higher levels of circuit functionality are tightly related to an emphasis on compactness in consumer electronic products and a widespread growth and interest in wireless communications and products. These trends are expected to persist for some time as technology and design methodologies continue to evolve and the era of Systems on a Chip has definitely come of age. While technology improvements and spiraling silicon capacity allow designers to pack more functions onto a single piece of silicon, they also highlight a pressing challenge for system designers to keep up with such amazing complexity. To handle higher operating speeds and the constraints of portability and connectivity, new circuit techniques have appeared. Intensive research and progress in EDA tools, design methodologies and techniques is required to empower designers with the ability to make efficient use of the potential offered by this increasing silicon capacity and complexity and to enable them to design, test, verify and build such systems.

This book constitutes the proceedings of the 34th IFIP WG 6.1 International Conference on Formal Techniques for Distributed Objects, Components and Systems, FORTE 2014, held in Berlin, Germany, in June 2014, as part of the 9th International Federated Conference on Distributed Computing Techniques, DisCoTec 2014. The 18 revised full papers presented were carefully reviewed and selected from 50 submissions. The papers present a wide range of topics on specification languages and type systems, monitoring and testing, security analysis and bisimulation, abstraction and reduction.

Despite its increasing importance, the verification and validation of the human-machine interface is perhaps the most overlooked aspect of system development. Although much has been written about the design and developmentprocess, very little organized information is available on how to verifyand validate highly complex and highly coupled dynamic systems. Inability toevaluate such systems adequately may become the limiting factor in our ability to employ systems that our technology and knowledge allow us to design. This volume, based on a NATO Advanced Science Institute held in 1992, is designed to provide guidance for the verification and validation of all highly complex and coupled systems. Air traffic control isused an an example to ensure that the theory is described in terms that will allow its implementation, but the results can be applied to all complex and coupled systems. The volume presents the knowledge and theory ina format that will allow readers from a wide variety of backgrounds to apply it to the systems for which they are responsible. The emphasis is on domains where significant advances have been made in the methods of identifying potential problems and in new testing methods and tools. Also emphasized are techniques to identify the assumptions on which a system is built and to spot their weaknesses.

APPLEPIES 2015

Hardware Verification with System Verilog

System-on-a-Chip Verification

Professional Verification

11th IFIP WG 10.5 Advanced Research Working Conference, CHARME 2001 Livingston, Scotland, UK, September 4-7, 2001 Proceedings

Intelligent Computing, Information and Control Systems

Verification and Validation of Complex Systems: Human Factors Issues