Synopsys Design Compiler User Guide

This book introduces readers to alternative approaches to designing efficient embedded systems using unconventional number systems. The authors describe various systems that can be used for designing efficient embedded and application-specific processors, such as Residue Number System, Logarithmic Number System, Redundant Binary Number System Double-Base Number System, Decimal Floating Point Number System and Continuous Valued Number System. Readers will learn the strategies and trade-offs of using unconventional number systems in application-specific processors and be able to apply and design appropriate arithmetic operations from these number systems to boost the performance of digital systems.

Logic Synthesis Using Synopsys®Springer Science & Business Media

Concurrent design, or co-design of hardware and software is extremely important for meeting design goals, such as high performance, that are the key to commercial competitiveness. Hardware/Software Co-Design covers many aspects of the subject, including methods and examples for designing: (1) general purpose and embedded computing systems based on instruction set processors; (2) telecommunication systems using general purpose digital signal processors as well as application specific instruction set processors; (3) embedded control systems and applications to automotive electronics. The book also surveys the areas of emulation and prototyping systems with field programmable gate array technologies, hardware/software synthesis and verification, and industrial design trends. Most contributions emphasize the design methodology, the requirements and state of the art of computer aided co-design tools, together with current design examples.

After a brief introduction to low-power VLSI design, the design space of ASIP instruction set architectures (ISAs) is introduced with a special focus on important features for digital signal processing. Based on the degrees of freedom offered by this design space, a consistent ASIP design flow is proposed: this design flow starts with a given application and uses incremental optimization of the ASIP hardware, of ASIP coprocessors and of the ASIP software by using a top-down approach and by applying application-specific modifications on all levels of design hierarchy. A broad range of real-world signal processing applications serves as vehicle to illustrate each design decision and provides a hands-on approach to ASIP design. Finally, two complete case studies demonstrate the feasibility and the efficiency of the proposed methodology and quantitatively evaluate the benefits of ASIPs in an industrial context.

Reliable Software for Unreliable Hardware

12th International Conference, Seoul, Korea, December 2-4. 2009. Revised Selected Papers

Cybernetics And Systems '94 - Proceedings Of The 12th European Meeting On Cybernetics And Systems Research (In 2 Volumes)

4th International Workshop, Ottawa, Ontario, May 16 - 20, 1994. Selected Papers
Design of Energy-Efficient Application-Specific Instruction Set Processors
Algorithms and VLSI Implementations of MIMO Detection

This highly relevant and up-to-the-minute book constitutes the refereed proceedings of the Third International Conference on High Performance Embedded Architectures and Compilers, HiPEAC 2008, held in Göteborg, Sweden, January 27-29, 2008. The 25 revised full papers presented together with 1 invited keynote paper were carefully reviewed and selected from 77 submissions. The papers are organized into topical sections on a number of key subjects in the field.

For those with a basic understanding of digital design, this book teaches the essential skills to design digital integrated circuits using Verilog and the relevant extensions of SystemVerilog. In addition to covering the syntax of Verilog and SystemVerilog, the author provides an appreciation of design challenges and solutions for producing working circuits. The book covers not only the syntax and limitations of HDL coding, but deals extensively with design problems such as partitioning and synchronization, helping you to produce designs that are not only logically correct, but will actually work when turned into physical circuits. Throughout the book, many small examples are used to validate concepts and demonstrate how to apply design skills. This book takes readers who have already learned the fundamentals of digital design to the point where they can produce working circuits using modern design methodologies. It clearly explains what is useful for circuit design and what parts of the languages are only software, providing a non-theoretical, practical guide to robust, reliable and optimized hardware design and development. Produce working hardware: Covers not only syntax, but also provides design know-how, addressing problems such as synchronization and partitioning to produce working solutions Usable examples: Numerous small examples throughout the book demonstrate concepts in an easy-to-grasp manner Essential knowledge: Covers the vital design topics of synchronization, essential for producing working silicon; asynchronous interfacing techniques; and design techniques for circuit optimization, including partitioning

This book constitutes the refereed proceedings of the 22nd International Conference on Architecture of Computing Systems, ARCS 2009, held in Delft, The Netherlands, in March 2009. The 21 revised full papers presented together with 3 keynote papers were carefully reviewed and selected from 57 submissions. This year's special focus is set on energy awareness. The papers are organized in topical sections on compilation technologies, reconfigurable hardware and applications, massive parallel architectures, organic computing, memory architectures, enery awareness, Java processing, and chip-level multiprocessing.

This book describes for readers a methodology for dynamic power estimation, using Transaction Level Modeling (TLM). The methodology exploits the existing tools for RTL simulation, design synthesis and SystemC prototyping to provide fast and accurate power estimation using Transaction Level Power Modeling (TLPM). Readers will benefit from this innovative way of evaluating power on a high level of abstraction, at an early stage of the product life cycle, decreasing the number of the expensive design iterations.

Electronic Design Automation for IC System Design, Verification, and Testing
Theory and Applications
Quantifying and Exploring the Gap Between FPGAs and ASICs
A Guide to Using SystemVerilog for Hardware Design and Modeling
Computational Science -- ICCS 2005
Digital Logic Design Using Verilog

"3-Dimensional VLSI: A 2.5-Dimensional Integration Scheme"elaborates the concept

and importance of 3-Dimensional (3-D) VLSI. The authors have developed a new 3-D IC integration paradigm, so-called 2.5-D integration, to address many problems that are hard to resolve using traditional non-monolithic integration schemes. The book also introduces major 3-D VLSI design issues that need to be solved by IC designers and Electronic Design Automation (EDA) developers. By treating 3-D integration in an integrated framework, the book provides important insights for semiconductor process engineers, IC designers, and those working in EDA R&D. Dr. Yangdong Deng is an associate professor at the Institute of Microelectronics, Tsinghua University, China. Dr. Wojciech P. Maly is the U. A. and Helen Whitaker Professor at the Department of Electrical and Computer Engineering, Carnegie Mellon University, USA.

This book describes new and effective methodologies for modeling, analyzing and mitigating cell-internal signal electromigration in nanoCMOS, with significant circuit lifetime improvements and no impact on performance, area and power. The authors are the first to analyze and propose a solution for the electromigration effects inside logic cells of a circuit. They show in this book that an interconnect inside a cell can fail reducing considerably the circuit lifetime and they demonstrate a methodology to optimize the lifetime of circuits, by placing the output, Vdd and Vss pin of the cells in the less critical regions, where the electromigration effects are reduced. Readers will be enabled to apply this methodology only for the critical cells in the circuit, avoiding impact in the circuit delay, area and performance, thus increasing the lifetime of the circuit without loss in other characteristics.

Logic Synthesis Using Synopsys ®, Second Edition is for anyone who hates reading manuals but would still like to learn logic synthesis as practised in the real world. Synopsys Design Compiler, the leading synthesis tool in the EDA marketplace, is the primary focus of the book. The contents of this book are specially organized to assist designers accustomed to schematic capture-based design to develop the required expertise to effectively use the Synopsys Design Compiler. Over 100 `Classic Scenarios' faced by designers when using the Design Compiler have been captured, discussed and solutions provided. These scenarios are based on both personal experiences and actual user queries. A general understanding of the problem-solving techniques provided should help the reader debug similar and more complicated problems. In addition, several examples and dc_shell scripts (Design Compiler scripts) have also been provided. Logic Synthesis Using Synopsys ®, Second Edition is an updated and revised version of the very successful first edition. The second edition covers several new and emerging areas, in addition to improvements in the presentation and contents in all chapters from the first edition. With the rapid shrinking of process geometries it is becoming increasingly important that `physical' phenomenon like clusters and wire loads be considered during the synthesis phase. The increasing demand for FPGAs has warranted a greater focus on FPGA synthesis tools and methodology. Finally, behavioral synthesis, the move to designing at a higher level of abstraction than RTL, is fast becoming a reality. These factors have resulted in the inclusion of separate chapters in the second edition to cover Links to Layout, FPGA Synthesis and Behavioral Synthesis, respectively. Logic Synthesis Using Synopsys ®, Second Edition has been written with the CAD engineer in mind. A clear understanding of the synthesis tool concepts, its capabilities and the related CAD issues will help the CAD engineer formulate an effective synthesis-based ASIC design methodology. The intent is also to assist design teams to better incorporate and effectively integrate synthesis with their existing in-house design methodology and CAD tools.

Dark Silicon and the Future of On-chip Systems, Volume 110, the latest release in the Advances in Computers series published since 1960, presents detailed coverage of innovations in computer hardware, software, theory, design and applications, with this release focusing on an Introduction to dark silicon and future processors, a Revisiting of processor allocation and application mapping in future CMPs in the dark silicon era, Multi-objectivism in the dark silicon age, Dark silicon aware resource management for many-core systems, Dynamic power management for dark silicon multi-core processors, Topology specialization for networks-on-chip in the dark silicon era, and Emerging SRAM-based FPGA architectures. Provides in-depth surveys and tutorials on new computer technology Covers well-known authors and researchers in the field Presents extensive bibliographies with most chapters Includes volumes that are devoted to single themes or subfields of computer science, with this release focusing on Dark Silicon and Future On-chip Systems

Transaction-Level Power Modeling

Ultra-Low Energy Domain-Specific Instruction-Set Processors

Advanced ASIC Chip Synthesis

12th International Workshop, Santa Barbara, USA, August 17-20,2010, Proceedings

Tools and Techniques for Low Power Design

MIMO Systems

This book describes novel software concepts to increase reliability under user-defined constraints. The authors' approach bridges, for the first time, the reliability gap between hardware and software. Readers will learn how to achieve increased soft error resilience on unreliable hardware, while exploiting the inherent error masking characteristics and error (stemming from soft errors, aging, and process variations) mitigations potential at different software layers.

This book provides a detailed overview of detection algorithms for multiple-input multiple-output (MIMO) communications systems focusing on their hardware realisation. The book begins by analysing the maximum likelihood detector, which provides the optimal bit error rate performance in an uncoded communications system. However, the maximum likelihood detector experiences a high complexity that scales exponentially with the number of antennas, which makes it impractical for real-time communications systems. The authors proceed to discuss lower-complexity detection algorithms such as zero-forcing, sphere decoding, and the K-best algorithm, with the aid of detailed algorithmic analysis and several MATLAB code examples. Furthermore, different design examples of MIMO detection algorithms and their hardware implementation results are presented and discussed. Finally, an ASIC design flow for implementing MIMO detection algorithms in hardware is provided, including the system simulation and modelling steps and register transfer level modelling using hardware description languages. Provides an overview of MIMO detection algorithms and discusses their corresponding hardware implementations in detail; Highlights architectural considerations of MIMO detectors in achieving low power consumption and high throughput; Discusses design tradeoffs that will guide readers' efforts when implementing MIMO algorithms in hardware; Describes a broad range of implementations of different MIMO detectors, enabling readers to make informed design decisions

based on their application requirements.

Compendio de los trabajos presentados en Toledo durante el VHDL user's forum in Europe.

The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook, Second Edition, Electronic Design Automation for IC System Design, Verification, and Testing thoroughly examines system-level design, microarchitectural design, logic verification, and testing. Chapters contributed by leading experts authoritatively discuss processor modeling and design tools, using performance metrics to select microprocessor cores for integrated circuit (IC) designs, design and verification languages, digital simulation, hardware acceleration and emulation, and much more. New to This Edition: Major updates appearing in the initial phases of the design flow, where the level of abstraction keeps rising to support more functionality with lower non-recurring engineering (NRE) costs Significant revisions reflected in the final phases of the design flow, where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting-edge applications and approaches realized in the decade since publication of the previous edition—these are illustrated by new chapters on high-level synthesis, system-on-chip (SoC) block-based design, and back-annotating system-level models Offering improved depth and modernity, Electronic Design Automation for IC System Design, Verification, and Testing provides a valuable, state-of-the-art reference for electronic design automation (EDA) students, researchers, and professionals.

Emerging Memory and Computing Devices in the Era of Intelligent Machines

Using Synopsys® Design CompilerTM and PrimeTime®

Introduction to Low-Power Design in VLSIs

Using Synopsys® Design CompilerTM Physical CompilerTM and PrimeTime®

VLSI-SoC: From Algorithms to Circuits and System-on-Chip Design

Reuse Methodology Manual for System-on-a-chip Designs

Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® and PrimeTime® describes the advanced concepts and techniques used for ASIC chip synthesis, formal verification and static timing analysis, using the Synopsys suite of tools. In addition, the entire ASIC design flow methodology targeted for VDSM (Very-Deep-Sub-Micron) technologies is covered in detail. The emphasis of this book is on real-time application of Synopsys tools used to combat various problems seen at VDSM geometries. Readers will be exposed to an effective design methodology for handling complex, sub-micron ASIC designs. Significance is placed on HDL coding styles, synthesis and optimization, dynamic simulation, formal verification, DFT scan insertion, links to layout, and static timing analysis. At each step, problems related to each phase of the design flow are identified, with solutions and work-arounds described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at length. Furthermore, the book contains in-depth discussions on the basics of

Synopsys technology libraries and HDL coding styles, targeted towards optimal synthesis solutions. Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® and PrimeTime® is intended for anyone who is involved in the ASIC design methodology, starting from RTL synthesis to final tape-out. Target audiences for this book are practicing ASIC design engineers and graduate students undertaking advanced courses in ASIC chip design and DFT techniques. From the Foreword: `This book, written by Himanshu Bhatnagar, provides a comprehensive overview of the ASIC design flow targeted for VDSM technologies using the Synopsis suite of tools. It emphasizes the practical issues faced by the semiconductor design engineer in terms of synthesis and the integration of front-end and back-end tools. Traditional design methodologies are challenged and unique solutions are offered to help define the next generation of ASIC design flows. The author provides numerous practical examples derived from real-world situations that will prove valuable to practicing ASIC design engineers as well as to students of advanced VLSI courses in ASIC design'. Dr Dwight W. Decker, Chairman and CEO, Conexant Systems, Inc., (Formerly, Rockwell Semiconductor Systems), Newport Beach, CA, USA.

Annotation This book constitutes the refereed proceedings of the 12th International Workshop on Cryptographic Hardware and Embedded Systems, CHES 2010, held in Santa Barbara, USA during August 17-20, 2010. This year it was co-located with the 30th International Cryptology Conference (CRYPTO). The book contains 2 invited talks and 30 revised full papers which were carefully reviewed and selected from from 108 submissions. The papers are organized in topical sections on low cost cryptography, efficient implementation, side-channel attacks and countermeasures, tamper resistance, hardware trojans, PUFs and RNGs.

Logic synthesis has become a fundamental component of the ASIC design flow, and Logic Synthesis Using Synopsys® has been written for all those who dislike reading manuals but who still like to learn logic synthesis as practised in the real world. The primary focus of the book is Synopsys Design Compiler®: the leading synthesis tool in the EDA marketplace. The book is specially organized to assist designers accustomed to schematic capture based design to develop the required expertise to effectively use the Compiler. Over 100 `classic scenarios' faced by designers using the Design Compiler have been captured and discussed, and solutions provided. The scenarios are based both on personal experiences and actual user queries. A general understanding of the problem-solving techniques provided will help the reader debug similar and more complicated problems. Furthermore, several examples and dc-shell scripts are provided. Specifically, Logic Synthesis Using Synopsys® will help the reader develop a better understanding of the synthesis design flow, optimization strategies using the Design Compiler, test insertion using the Test Compiler®, commonly used interface formats such as EDIF and SDF, and design re-use in a synthesis-based design methodology. Examples have been provided in both VHDL and Verilog. Audience: Written with CAD engineers in mind to enable them to formulate an effective synthesis-

based ASIC design methodology. Will also assist design teams to better incorporate and effectively integrate synthesis with their existing in-house design methodology and CAD tools.

This book offers the first comprehensive coverage of digital design techniques to expand the power-performance tradeoff well beyond that allowed by conventional wide voltage scaling. Compared to conventional fixed designs, the approach described in this book makes digital circuits more versatile and adaptive, allowing simultaneous optimization at both ends of the power-performance spectrum. Drop-in solutions for fully automated and low-effort design based on commercial CAD tools are discussed extensively for processors, accelerators and on-chip memories, and are applicable to prominent applications (e.g., IoT, AI, wearables, biomedical). Through the higher power-performance versatility techniques described in this book, readers are enabled to reduce the design effort through reuse of the same digital design instance, across a wide range of applications. All concepts the authors discuss are demonstrated by dedicated testchip designs and experimental results. To make the results immediately usable by the reader, all the scripts necessary to create automated design flows based on commercial tools are provided and explained.

Third International Conference, HiPEAC 2008, Göteborg, Sweden, January 27-29, 2008, Proceedings

15th International Workshop, PATMOS 2005, Leuven, Belgium, September 21-23, 2005, Proceedings

13th International Workshop, PATMOS 2003, Torino, Italy, September 10-12, 2003, Proceedings

Cryptographic Hardware and Embedded Systems -- CHES 2010

Dark Silicon and Future On-chip Systems

Computer Aided Systems Theory - CAST '94

Advanced ASIC Chip Synthesis: Using Synopsys ® Design Compiler ® Physical Compiler ® and PrimeTime ® , Second Edition describes the advanced concepts and techniques used towards ASIC chip synthesis, physical synthesis, formal verification and static timing analysis, using the Synopsys suite of tools. In addition, the entire ASIC design flow methodology targeted for VDSM (Very-Deep-Sub-Micron) technologies is covered in detail. The emphasis of this book is on real-time application of Synopsys tools, used to combat various problems seen at VDSM geometries. Readers will be exposed to an effective design methodology for handling complex, sub-micron ASIC designs. Significance is placed on HDL coding styles, synthesis and optimization, dynamic simulation, formal verification, DFT scan insertion, links to layout, physical synthesis, and static timing analysis. At each step, problems related to each phase of the design flow are identified, with solutions and work-around described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at length. Furthermore, the book contains in-depth discussions on the basis of Synopsys technology libraries and HDL coding styles, targeted towards optimal synthesis solution. Target audiences

for this book are practicing ASIC design engineers and masters level students undertaking advanced VLSI courses on ASIC chip design and DFT techniques.
This book constitutes thoroughly refereed post-conference proceedings of the workshops of the 19th International Conference on Parallel Computing, Euro-Par 2013, held in Aachen, Germany in August 2013. The 99 papers presented were carefully reviewed and selected from 145 submissions. The papers include seven workshops that have been co-located with Euro-Par in the previous years: - Big Data Cloud (Second Workshop on Big Data Management in Clouds) - Hetero Par (11th Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms) - HiBB (Fourth Workshop on High Performance Bioinformatics and Biomedicine) - OMHI (Second Workshop on On-chip Memory Hierarchies and Interconnects) - PROPER (Sixth Workshop on Productivity and Performance) - Resilience (Sixth Workshop on Resiliency in High Performance Computing with Clusters, Clouds, and Grids) - UCHPC (Sixth Workshop on Un Conventional High Performance Computing) as well as six newcomers: - DIHC (First Workshop on Dependability and Interoperability in Heterogeneous Clouds) - Fed ICI (First Workshop on Federative and Interoperable Cloud Infrastructures) - LSDVE (First Workshop on Large Scale Distributed Virtual Environments on Clouds and P2P) - MHPC (Workshop on Middleware for HPC and Big Data Systems) -PADABS (First Workshop on Parallel and Distributed Agent Based Simulations) - ROME (First Workshop on Runtime and Operating Systems for the Many core Era) All these workshops focus on promotion and advancement of all aspects of parallel and distributed computing.
Welcome to the proceedings of PATMOS 2003. This was the 13th in a series of international workshops held in several locations in Europe. Over the years, PATMOS has gained recognition as one of the major European events devoted to power and timing aspects of integrated circuit and system design. Despite its signi?cant growth and development, PATMOS can still be considered as a very informal forum, featuring high-level scienti?c presentations together with open discussions and panel sessions in a free and relaxed environment. This year, PATMOS took place in Turin, Italy, organized by the Politecnico di Torino, with technical co-sponsorship from the IEEE Circuits and Systems Society and the generous support of the European Commission, as well as that of several industrial sponsors, including BullDAST, Cadence, Mentor Graphics, STMicroelectronics, and Synopsys. The objective of the PATMOS workshop is to provide a forum to discuss and investigate the emerging problems in methodologies and tools for the design of new generations of integrated circuits and systems. A major emphasis of the technical program is on speed and low-power aspects, with particular regard to modeling, characterization, design, and architectures.
This book contains extended and revised versions of the best papers presented at the 20th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2012, held in Santa Cruz, CA, USA, in October 2012. The

12 papers included in the book were carefully reviewed and selected from the 33 full papers presented at the conference. The papers cover a wide range of topics in VLSI technology and advanced research. They address the current trend toward increasing chip integration and technology process advancements bringing about stimulating new challenges both at the physical and system-design levels, as well as in the test of these systems.

Design and Modeling of Low Power VLSI Systems

High-Quality Delay Tests

Digital Integrated Circuit Design Using Verilog and Systemverilog

From the Clock Path to the Data Path

Euro-Par 2013: Parallel Processing Workshops

The Fifth International Conference on Computational Science (ICCS 2005) held in Atlanta, Georgia, USA, May 22–25, 2005, continued in the tradition of p- vious conferences in the series: ICCS 2004 in Krakow, Poland; ICCS 2003 held simultaneously at two locations, in Melbourne, Australia and St. Petersburg, Russia; ICCS 2002 in Amsterdam, The Netherlands; and ICCS 2001 in San Francisco, California, USA. Computational science is rapidly maturing as a mainstream discipline. It is central to an ever-expanding variety of ?elds in which computational methods and tools enable new discoveries with greater accuracy and speed. ICCS 2005 waso rganizedasaforumforscientistsfromthecorediscipli nesofcomputational science and numerous application areas to discuss and exchange ideas, results, and future directions. ICCS participants included researchers from many app- cation domains, including those interested in advanced computational methods for physics, chemistry, life sciences, engineering, economics and ?nance, arts and humanities, as well as computer system vendors and software developers. The primary objectives of this conference were to discuss problems and solutions in allareas,toidentifyn ewissues,toshapefuturedirectionsofresearch,andtohelp users apply various advanced computational techniques. The event highlighted recent developments in algorithms, computational kernels, next generation c- puting systems, tools, advanced numerical methods, data-driven systems, and emerging application ?elds, such as complex systems, ?nance, bioinformatics, computational aspects of wireless and mobile networks, graphics, and hybrid computation.

This book provides some recent advances in design nanometer VLSI chips. The selected topics try to present some open problems and challenges with important topics ranging from design tools, new post-silicon devices, GPU-based parallel computing, emerging 3D integration, and antenna design. The book consists of two parts, with chapters such as: VLSI design for multi-sensor smart systems on a chip, Three-dimensional integrated circuits design for thousand-core processors, Parallel symbolic analysis of large analog circuits on GPU platforms, Algorithms for CAD tools VLSI design, A multilevel memetic algorithm for large SAT-encoded problems, etc.

SystemVerilog is a rich set of extensions to the IEEE 1364-2001 Verilog Hardware Description Language (Verilog HDL). These extensions address

two major aspects of HDL based design. First, modeling very large designs with concise, accurate, and intuitive code. Second, writing high-level test programs to efficiently and effectively verify these large designs. This book, SystemVerilog for Design, addresses the first aspect of the SystemVerilog extensions to Verilog. Important modeling features are presented, such as two-state data types, enumerated types, user-defined types, structures, unions, and interfaces. Emphasis is placed on the proper usage of these enhancements for simulation and synthesis. A companion to this book, SystemVerilog for Verification, covers the second aspect of SystemVerilog.

Field-programmable gate arrays (FPGAs), which are pre-fabricated, programmable digital integrated circuits (ICs), provide easy access to state-of-the-art integrated circuit process technology, and in doing so, democratize this technology of our time. This book is about comparing the qualities of FPGA – their speed performance, area and power consumption, against custom-fabricated ICs, and exploring ways of mitigating their de ciencies. This work began as a question that many have asked, and few had the resources to answer – how much worse is an FPGA compared to a custom-designed chip? As we dealt with that question, we found that it was far more dif cult to answer than we anticipated, but that the results were rich basic insights on fundamental understandings of FPGA architecture. It also encouraged us to nd ways to leverage those insights to seek ways to make FPGA technology better, which is what the second half of the book is about. While the question "How much worse is an FPGA than an ASIC?" has been a constant sub-theme of all research on FPGAs, it was posed most directly, some time around May 2004, by Professor Abbas El Gamal from Stanford University to us – he was working on a 3D FPGA, and was wondering if any real measurements had been made in this kind of comparison. Shortly thereafter we took it up and tried to answer in a serious way.

Architecture of Computing Systems - ARCS 2009

VLSI Design

22nd International Conference, Delft, The Netherlands, March 10-13, 2009, Proceedings

A 2.5-Dimensional Integration Scheme

High Performance Embedded Architectures and Compilers

A Cross Layer Perspective

This second edition focuses on the thought process of digital design and implementation in the context of VLSI and system design. It covers the Verilog 2001 and Verilog 2005 RTL design styles, constructs and the optimization at the RTL and synthesis level. The book also covers the logic synthesis, low power, multiple clock domain design concepts and design performance improvement techniques. The book includes 250 design examples/illustrations and 100 exercise questions. This volume can be used as a core or supplementary text in undergraduate courses on logic design and as a text for professional and vocational coursework. In addition, it will be a hands-on professional reference and a self-study aid for hobbyists.

Computing systems are undergoing a transformation from logic-centric towards memory-centric architectures, where overall performance and energy efficiency at the system level are determined by the density, performance, functionality and efficiency of the memory, rather than the logic sub-system. This is driven by the requirements of data-intensive applications in artificial intelligence, autonomous systems, and edge computing. We are at an exciting time in the semiconductor industry where several innovative device and technology concepts are being developed to respond to these demands, and capture shares of the fast growing market for AI-related hardware. This special issue is devoted to highlighting, discussing and presenting the latest advancements in this area, drawing on the best work on emerging memory devices including magnetic, resistive, phase change, and other types of memory. The special issue is interested in work that presents concepts, ideas, and recent progress ranging from materials, to memory devices, physics of switching mechanisms, circuits, and system applications, as well as progress in modeling and design tools. Contributions that bridge across several of these layers are especially encouraged.

Very Large Scale Integration (VLSI) Systems refer to the latest development in computer microchips which are created by integrating hundreds of thousands of transistors into one chip. Emerging research in this area has the potential to uncover further applications for VSLI technologies in addition to system advancements. Design and Modeling of Low Power VLSI Systems analyzes various traditional and modern low power techniques for integrated circuit design in addition to the limiting factors of existing techniques and methods for optimization. Through a research-based discussion of the technicalities involved in the VLSI hardware development process cycle, this book is a useful resource for researchers, engineers, and graduate-level students in computer science and engineering.

Modern consumers carry many electronic devices, like a mobile phone, digital camera, GPS, PDA and an MP3 player. The functionality of each of these devices has gone through an important evolution over recent years, with a steep increase in both the number of features as in the quality of the services that they provide. However, providing the required compute power to support (an uncompromised combination of) all this functionality is highly non-trivial. Designing processors that meet the demanding requirements of future mobile devices requires the optimization of the embedded system in general and of the embedded processors in particular, as they should strike the correct balance between flexibility, energy efficiency and performance. In general, a designer will try to minimize the energy consumption (as far as needed) for a given performance, with a sufficient flexibility. However, achieving this goal is

already complex when looking at the processor in isolation, but, in reality, the processor is a single component in a more complex system. In order to design such complex system successfully, critical decisions during the design of each individual component should take into account effect on the other parts, with a clear goal to move to a global Pareto optimum in the complete multi-dimensional exploration space. In the complex, global design of battery-operated embedded systems, the focus of Ultra-Low Energy Domain-Specific Instruction-Set Processors is on the energy-aware architecture exploration of domain-specific instruction-set processors and the co-optimization of the datapath architecture, foreground memory, and instruction memory organisation with a link to the required mapping techniques or compiler steps at the early stages of the design. By performing an extensive energy breakdown experiment for a complete embedded platform, both energy and performance bottlenecks have been identified, together with the important relations between the different components. Based on this knowledge, architecture extensions are proposed for all the bottlenecks.

20th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2012, Santa Cruz, CA, USA, October 7-10, 2012, Revised Selected Papers

Logic Synthesis Using Synopsys®

Electromigration Inside Logic Cells

VHDL User's Forum in Europe

Modeling, Analyzing and Mitigating Signal Electromigration in NanoCMOS

Hardware/Software Co-Design

This volume presents a collection of revised refereed papers selected from the presentations at the Fourth International Workshop on Computer Aided Systems Theory - CAST '94, held in Ottawa, Ontario, Canada in May 1994. The 31 full papers included in the book were chosen from originally 82 submissions and reflect the state of the art in the area of computer aided systems theory. The volume is divided into sections on foundations, methods, and tools and environments.

Explains how to use low power design in an automated design flow, and examine the design time and performance trade-offs Includes the latest tools and techniques for low power design applied in an ASIC design flow Focuses on low power in an automated design methodology, a much neglected area

In recent years, it was realized that the MIMO communication systems seems to be inevitable in accelerated evolution of high data rates applications due to their potential to dramatically increase the spectral efficiency and simultaneously sending individual information to the corresponding users in wireless systems. This book, intends to provide highlights of the current

research topics in the field of MIMO system, to offer a snapshot of the recent advances and major issues faced today by the researchers in the MIMO related areas. The book is written by specialists working in universities and research centers all over the world to cover the fundamental principles and main advanced topics on high data rates wireless communications systems over MIMO channels. Moreover, the book has the advantage of providing a collection of applications that are completely independent and self-contained; thus, the interested reader can choose any chapter and skip to another without losing continuity.

Silicon technology now allows us to build chips consisting of tens of millions of transistors. This technology not only promises new levels of system integration onto a single chip, but also presents significant challenges to the chip designer. As a result, many ASIC developers and silicon vendors are re-examining their design methodologies, searching for ways to make effective use of the huge numbers of gates now available. Design reuse -- the use of pre-designed and pre-verified cores -- is the most promising opportunity to bridge the gap between available gate-count and designer productivity. Reuse Methodology Manual for System-On-A-Chip Designs, Second Edition outlines an effective methodology for creating reusable designs for use in a System-on-a-Chip (SoC) design methodology. Silicon and tool technologies move so quickly that no singlemethodology can provide a permanent solution to this highly dynamic problem. Instead, this manual is an attempt to capture and incrementally improve on current best practices in the industry, and to give a coherent, integrated view of the design process.

Information Security and Cryptology - ICISC 2009

Nanometer Technology Designs

Closing the Power Gap between ASIC & Custom

BigDataCloud, DIHC, FedICI, HeteroPar, HiBB, LSDVE, MHPC, OMHI, PADABS, PROPER, Resilience, ROME, UCHPC 2013, Aachen, Germany, August 26-30, 2013. Revised Selected Papers

SystemVerilog For Design

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation

This book constitutes the proceedings of the 12th International Conference on Information Security and Cryptology, held in Seoul, Korea, in December 2009.

Traditional at-speed test methods cannot guarantee high quality test results as they face many new challenges. Supply noise effects on chip performance, high test pattern volume, small delay defect test pattern generation, high cost of test implementation and application, and utilizing low-cost testers are among these challenges. This book discusses these

challenges in detail and proposes new techniques and methodologies to improve the overall quality of the transition fault test.

This book constitutes the refereed proceedings of the 15th International Workshop on Power and Timing Optimization and Simulation, PATMOS 2005, held in Leuven, Belgium in September 2005. The 74 revised full papers presented were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on low-power processors, code optimization for low-power, high-level design, telecommunications and signal processing, low-power circuits, system-on-chip design, busses and interconnections, modeling, design automation, low-power techniques, memory and register files, applications, digital circuits, and analog and physical design.

3-Dimensional VLSI

Coding and RTL Synthesis

Embedded Systems Design with Special Arithmetic and Number Systems

Adaptive Digital Circuits for Power-Performance Range beyond Wide Voltage Scaling

5th International Conference, Atlanta, GA, USA, May 22-25, 2005, Proceedings, Part I