Intel Compiler Optimization Guide

The 6th International Conference on Computational and Information Sciences (ICCIS2014) will be held in NanChong, China. The 6th International Conference on Computational and Information Sciences (ICCIS2014)aims at bringing researchers in the areas of computational and information sciences to exchange new ideas and to explore new ground. The goal of the conference is to push the application of modern computing technologies to science, engineering, and information technologies.Following the success of ICCIS2004,ICCIS2010 and ICCIS2011,ICCIS2012,ICCIS2013,ICCIS2014 conference will consist of invited keynote presentations and contributed presentations of latest developments in computational and information sciences. The 2014 International Conference on Computational and Information Sciences (ICCIS 2014), now in its sixth run, has become one of the premier conferences in this dynamic and exciting field. The goal of ICCIS is to catalyze the communications among various communities in computational and information sciences. ICCIS provides a venue for the participants to share their recent research and development, to seek for collaboration resources and opportunities, and to build professional networks.

Provides information on how computer systems operate, how compilers work, and writing source code.

Android on x86: an Introduction to Optimizing for Intel® Architecture serves two main purposes. First, it makes the case for adapting your applications onto Intel's x86 architecture, including discussions of the business potential, the changing landscape of the Android marketplace, and the unique challenges and opportunities that arise from x86 devices. The fundamental idea is that extending your applications to support x86 or creating new ones is not difficult, but it is imperative to know all of the technicalities. This book is dedicated to providing you with an awareness of these nuances and an understanding of how to tackle them. Second, and most importantly, this book provides a one-stop detailed resource for best practices and procedures associated with the installation issues, hardware optimization issues, software requirements, programming tasks, and performance optimizations that emerge when developers consider the x86 Android devices. Optimization discussions dive into native code, hardware acceleration, and advanced profiling of multimedia applications. The authors have collected this information so that you can use the book as a guide for the specific requirements of each application project. This book is not dedicated solely to code; instead it is filled with the information you need in order to take advantage of x86 architecture. It will guide you through installing the Android SDK for Intel Architecture, help you understand the differences and similarities between processor architectures available in Android devices, teach you to create and port applications, debug existing x86 applications, offer solutions for NDK and C++ optimizations, and introduce the Intel Hardware Accelerated Execution Manager. This book provides the most useful information to help you get the job done quickly while utilizing best practices.

Authors Jim Jeffers and James Reinders spent two years helping educate customers about the prototype and pre-production hardware before Intel introduced the first Intel Xeon Phi coprocessor. They have distilled their own experiences coupled with insights from many expert customers, Intel Field Engineers, Application Engineers and Technical Consulting Engineers, to create this authoritative first book on the essentials of programming for this new architecture and these new products. This book is useful even before you ever touch a system with an Intel Xeon Phi coprocessor. To ensure that your applications run at maximum efficiency, the authors emphasize key techniques for programming any modern parallel computing system whether based on Intel Xeon processors, Intel Xeon Phi coprocessors, or other high performance microprocessors. Applying these techniques will generally increase your program performance on any system, and better prepare you for Intel Xeon Phi coprocessors and the Intel MIC architecture. A practical guide to the essentials of the Intel Xeon Phi coprocessor Presents best practices for portable, high-performance computing and a familiar and proven threaded, scalar-vector programming model Includes simple but informative code examples that explain the unique aspects of this new highly parallel and high performance computational product Covers wide vectors, many cores, many threads and high bandwidth cache/memory architecture

Hacker's Delight

4th International Workshop, LightSec 2015, Bochum, Germany, September 10-11, 2015, Revised Selected Papers

Performance Analysis and Tuning on Modern CPUs

Multicore and Many-core Programming Approaches

Optimizing HPC Applications with Intel Cluster Tools

High-Performance Scientific Computing

Algorithms and Applications

This book constitutes the refereed proceedings of the 10th International Conference on Cryptology in India, INDOCRYPT 2009, held in New Dehli, India, in December 2009. The 28 revised full papers were carefully reviewed and selected from 104 submissions. The papers are organized in topical sections on post-quantum cryptology, key agreement protocols, side channel attacks, symmetric cryptology, hash functions, number theoretic cryptology, lightweight cryptology, signature protocols, and multiparty computation.

Coding and testing are often considered separate areas of expertise. In this comprehensive guide, author and Java expert Scott Oaks takes the approach that anyone who works with Java should be equally adept at understanding how code behaves in the JVM, as well as the tunings likely to help its performance. You'll gain in-depth knowledge of Java application performance, using the Java Virtual Machine (JVM) and the Java platform, including the language and API. Developers and performance engineers alike will learn a variety of features, tools, and processes for improving the way Java 7 and 8 applications perform. Apply four principles for obtaining the best results from performance testing Use JDK tools to collect data on how a Java application is performing Understand the advantages and disadvantages of using a JIT compiler Tune JVM garbage collectors to affect programs as little as possible Use techniques to manage heap memory and JVM native memory Maximize Java threading and synchronization performance features Tackle performance issues in Java EE and Java SE APIs Improve Java-driven database application performance

This is Volume I of the four-volume set LNCS 3991-3994 constituting the refereed proceedings of the 6th International Conference on Computational Science, ICCS 2006. The 98 revised full papers and 29 revised poster papers of the main track presented together with 500 accepted workshop papers were carefully reviewed and selected for inclusion in the four volumes. The coverage spans the whole range of computational science.

This Special Issue provides an opportunity for researchers in the area of side-channel attacks (SCAs) to highlight the most recent exciting technologies. The research papers published in this Special Issue represent recent progress in the field, including research on power analysis attacks, cache-based timing attacks, system-level countermeasures, and so on.

Thinking Low-Level, Writing High-Level

High Performance Computing

Side Channel Attacks

25th International Conference, FC 2021, Virtual Event, March 1–5, 2021, Revised Selected Papers, Part I

How to Fully Exploit MIC Architectures

22nd International Workshop, LCPC 2009, Newark, DE, USA, October 8-10, 2009, Revised Selected Papers

Hunting Petaflops

This book constitutes the refereed proceedings of the 20th International Conference on Integrated Circuit and System Design, PATMOS 2010, held in Grenoble, France, in September 2010. The 24 revised full papers presented and the 9 extended abstracts were carefully reviewed and are organized in topical sections on design flows; circuit techniques; low power circuits; self-timed circuits; process variation; high-level modeling of poweraware heterogeneous designs in SystemC-AMS; and minalogic.

Step-by-step guide to assembly language for the 64-bit Itanium processors, with extensive examples Details of Explicitly Parallel Instruction Computing (EPIC): Instruction set, addressing, register stack engine, predication, I/O, procedure calls, floating-point operations, and more Learn how to comprehend and optimize open source, Intel, and HP-UX compiler output Understand the full power of 64-bit Itanium EPIC processors Itanium(R) Architecture for Programmers is a comprehensive introduction to the breakthrough capabilities of the new 64-bit Itanium architecture. Using standard command-line tools and extensive examples, the authors illuminate the Itanium design within the broader context of contemporary computer architecture via a step-by-step investigation of Itanium assembly language. Coverage includes: The potential of Explicitly Parallel Instruction Computing (EPIC) Itanium instruction formats and addressing modes Innovations such as the register stack engine (RSE) and extensive predication Procedure calls and procedure-calling mechanisms Floating-point operations I/O techniques, from simple debugging to the use of files Optimization of output from open source, Intel, and HP-UX compilers An essential resource for both computing professionals and students of architecture or assembly language, Itanium Architecture for Programmers includes extensive printed and Web-based references, plus many numeric, essay, and programming exercises for each chapter.

This book is an all-in-one source of information for programming the Second-Generation Intel Xeon Phi product family also called Knights Landing. The authors provide detailed and timely Knights Landingspecific details, programming advice, and real-world examples. The authors distill their years of Xeon Phi programming experience coupled with insights from many expert customers — Intel Field Engineers, Application Engineers, and Technical Consulting Engineers — to create this authoritative book on the essentials of programming for Intel Xeon Phi products. Intel® Xeon PhiTM Processor High-Performance Programming is useful even before you ever program a system with an Intel Xeon Phi processor. To help ensure that your applications run at maximum efficiency, the authors emphasize key techniques for programming any modern parallel computing system whether based on Intel Xeon processors, Intel Xeon Phi processors, or other high-performance microprocessors. Applying these techniques will generally increase your program performance on any system and prepare you better for Intel Xeon Phi processors. A practical guide to the essentials for programming Intel Xeon Phi processors Definitive coverage of the Knights Landing architecture Presents best practices for portable, high-performance computing and a familiar and proven threads and vectors programming model Includes real world code examples that highlight usages of the unique aspects of this new highly parallel and high-performance computational product Covers use of MCDRAM, AVX-512, Intel® Omni-Path fabric, many-cores (up to 72), and many threads (4 per core) Covers software developer tools, libraries and programming models Covers using Knights Landing as a processor and a coprocessor

In today's fast and competitive world, a program's performance is just as important to customers as the features it provides. This practical guide teaches developers performance-tuning principles that enable optimization in C++. You'll learn how to make code that already embodies best practices of C++ design run faster and consume fewer resources on any computer--whether it's a watch, phone, workstation, supercomputer, or globe-spanning network of servers. Author Kurt Guntheroth provides several running examples that demonstrate how to apply these principles incrementally to improve existing code so it meets customer requirements for responsiveness and throughput. The advice in this book will prove itself the first time you hear a colleague exclaim, "Wow, that was fast. Who fixed something?"Locate performance hot spots using the profiler and software timersLearn to perform repeatable experiments to measure performance of code changesOptimize use of dynamically allocated variablesImprove performance of hot loops and functionsSpeed up string handling functionsRecognize efficient algorithms and optimization patternsLearn the strengths--and weaknesses--of C++ container classesView searching and sorting through an optimizer's eyeMake efficient use of C++ streaming I/O functionsUse C++ thread-based concurrency features effectively

Proven Techniques for Heightened Performance

Guide to Elliptic Curve Cryptography

From Supercomputing Competition to the Next HPC Generation

20th International Workshop, PATMOS 2010, Grenoble, France, September 7-10, 2010, Revised Selected Papers

Android on x86

Windows 2000 Performance Guide

Itanium Architecture for Programmers

"Presents the latest developments in the prgramming and design of programmable digital signal processors (PDSPs) with very-long-instruction word (VLIW) architecture, algorithm formulation and implementation, and modern applications for multimedia processing, communications, and industrial control."

This book constitutes the refereed proceedings of the 14th International Conference on Compiler Construction, CC 2005, held in Edinburgh, UK in April 2005 as part of ETAPS. The 21 revised full papers presented together with the extended abstract of an invited paper were carefully reviewed and selected from 91 submissions. The papers are organized in topical sections on compilation, parallelism, memory management, program transformation, tool demonstrations, and pointer analysis.

After two decades of research and development, elliptic curve cryptography now has widespread exposure and acceptance. Industry, banking, and government standards are in place to facilitate extensive deployment of this efficient public-key mechanism. Anchored by a comprehensive treatment of the practical aspects of elliptic curve cryptography (ECC), this guide explains the basic mathematics, describes state-of-the-art implementation methods, and presents standardized protocols for public-key encryption, digital signatures, and key establishment. In addition, the book addresses some issues that arise in software and hardware implementation, as well as side-channel attacks and countermeasures. Readers receive the theoretical fundamentals as an underpinning for a wealth of practical and accessible knowledge about efficient application. Features & Benefits: * Breadth of coverage and unified, integrated approach to elliptic curve cryptosystems * Describes important industry and government protocols, such as the FIPS 186-2 standard from the U.S. National Institute for Standards and Technology * Provides full exposition on techniques for efficiently implementing finite-field and elliptic curve arithmetic * Distills complex mathematics and algorithms for easy understanding * Includes useful literature references, a list of algorithms, and appendices on sample parameters, ECC standards, and software tools This comprehensive, highly focused reference is a useful and indispensable resource for practitioners, professionals, or researchers in computer science, computer engineering, network design, and network data security.

Performance tuning is becoming more important than it has been for the last 40 years. Read this book to understand your application's performance that runs on a modern CPU and learn how you can improve it. The 170+ page guide combines the knowledge of many optimization experts from different industries.

An Illustrated Introduction to Microprocessors and Computer Architecture

The Student Supercomputer Challenge Guide

A Practical Guide Using Embedded Intel Architecture

Intel Xeon Phi Coprocessor Architecture and Tools

International Conference on Computational and Information Sciences (ICCIS) 2014

Architecture: Programming, and Applications

Write Great Code, Volume 2

Intel® Xeon PhiTM Coprocessor Architecture and Tools: The Guide for Application Developers provides developers a comprehensive introduction and in-depth look at the Intel Xeon Phi coprocessor architecture and the corresponding parallel data structure tools and algorithms used in the various technical computing applications for which it is suitable. It also examines the source code-level optimizations that can be performed to exploit the powerful features of the processor. Xeon Phi is at the heart of world's fastest commercial supercomputer, which thanks to the massively parallel computing capabilities of Intel Xeon Phi processors coupled with Xeon Phi coprocessors attained 33.86 teraflops of benchmark performance in 2013. Extracting such stellar performance in real-world applications requires a sophisticated understanding of the complex interaction among hardware components, Xeon Phi cores, and the applications running on them. In this book, Rezaur Rahman, an Intel leader in the development of the Xeon Phi coprocessor and the optimization of its applications, presents and details all the features of Xeon Phi core design that are relevant to the practice of application developers, such as its vector units, hardware multithreading, cache hierarchy, and host-to-coprocessor communication channels. Building on this foundation, he shows developers how to solve real-world technical computing problems by selecting, deploying, and optimizing the available algorithms and data structure alternatives matching Xeon Phi's hardware characteristics. From Rahman's practical descriptions and extensive code examples, the reader will gain a working knowledge of the Xeon Phi vector instruction set and the Xeon Phi microarchitecture whereby cores execute 512-bit instruction streams in parallel.

The aim of this book is to explain to high-performance computing (HPC) developers how to utilize the Intel® Xeon PhiTM series products efficiently. To that end, it introduces some computing grammar, programming technology and optimization methods for using many-integrated-core (MIC) platforms and also offers tips and tricks for actual use, based on the authors' first-hand optimization experience. The material is organized in three sections. The first section, "Basics of MIC", introduces the fundamentals of MIC architecture and programming, including the specific Intel MIC programming environment. Next, the section on "Performance Optimization" explains general MIC optimization techniques, which are then illustrated step-by-step using the classical parallel programming example of matrix multiplication. Finally, "Project development" presents a set of practical and experience-driven methods for using parallel computing in application projects, including how to determine if a serial or parallel CPU program is suitable for MIC and how to transplant a program onto MIC. This book appeals to two main audiences: First, software developers for HPC applications – it will enable them to fully exploit the MIC architecture and thus achieve the extreme performance usually required in biological genetics, medical imaging, aerospace, meteorology and other areas of HPC. Second, students and researchers engaged in parallel and high-performance computing – it will guide them on how to push the limits of system performance for HPC applications.

Compiles programming hacks intended to help computer programmers build more efficient software, in an updated edition that covers cyclic redundancy checking and new algorithms and that includes exercises with answers.

This book introduces the state-of-the-art in research in parallel and distributed embedded systems, which have been enabled by developments in silicon technology, micro-electro-mechanical systems (MEMS), wireless communications, computer networking, and digital electronics. These systems have diverse applications in domains including military and defense, medical, automotive, and unmanned autonomous vehicles. The emphasis of the book is on the modeling and optimization of emerging parallel and distributed embedded systems in relation to the three key design metrics of performance, power and dependability. Key features: Includes an embedded wireless sensor networks case study to help illustrate the modeling and optimization of distributed embedded systems. Provides an analysis of multi-core/many-core based embedded systems to explain the modeling and optimization of parallel embedded systems. Features an application metrics estimation model; Markov modeling for fault tolerance and analysis; and queueing theoretic modeling for performance evaluation. Discusses optimization approaches for distributed wireless sensor networks; high-performance and energy-efficient techniques at the architecture, middleware and software levels for parallel multicore-based embedded systems; and dynamic optimization methodologies. Highlights research challenges and future research directions. The book is primarily aimed at researchers in embedded systems; however, it will also serve as an invaluable reference to senior undergraduate and graduate students with an interest in embedded systems research.

OpenMP: Portable Multi-Level Parallelism on Modern Systems

Getting the Most Out of Your Code

An Introduction to Optimizing for Intel Architecture

Data Parallel C++

Compiler Construction

Power and Performance

Lightweight Cryptography for Security and Privacy

Learn how to accelerate C++ programs using data parallelism. This open access book enables C++ programmers to be at the forefront of this exciting and important new development that is helping to push computing to new levels. It is full of practical advice, detailed explanations, and code examples to illustrate key topics. Data parallelism in C++ enables access to parallel resources in a modern heterogeneous system, freeing you from being locked into any particular computing device. Now a single C++ application can use any combination

of devices—including GPUs, CPUs, FPGAs and AI ASICs—that are suitable to the problems at hand. This book begins by introducing data parallelism and foundational topics for effective use of the SYCL standard from the Khronos Group and Data Parallel C++ (DPC++), the open source compiler used in this book. Later chapters cover advanced topics including error handling, hardware-specific programming, communication and synchronization, and memory model considerations. Data Parallel C++ provides you with everything needed to use SYCL for programming heterogeneous systems. What You'll Learn Accelerate C++ programs using data-parallel programming Target multiple device types (e.g. CPU, GPU, FPGA) Use SYCL and SYCL compilers Connect with computing's heterogeneous future via Intel's oneAPI initiative Who This Book Is For Those new data-parallel programming and computer programmers interested in data-parallel programming using C++.

Itisourpleasuretopresentthepapersacceptedforthe22ndInternationalWo- shop on Languages and Compilers for Parallel Computing held during October 8–10 2009 in Newark Delaware, USA. Since 1986, LCPC has became a valuable venueforresearchersto reportonworkinthegeneralareaofparallelcomputing, high-performance computer architecture and compilers. LCPC 2009 continued this tradition and in particular extended the area of interest to new parallel computing accelerators such as the IBM Cell Processor and Graphic Processing Unit (GPU). This year we received 52 submissions from 15 countries. Each submission receivedatleastthreereviewsandmosthadfour.ThePCalsosoughtadditional externalreviewsforcontentiouspapers.ThePCheldanall-dayphoneconference on August 24 to discuss the papers. PC members who had a con?ict of interest were asked to leave the call temporarily when the corresponding papers were discussed. From the 52 submissions, the PC selected 25 full papers and 5 short paperstobeincludedintheworkshopproceeding,representinga58%acceptance rate. We were fortunate to have three keynote speeches, a panel discussion and a tutorial in this year's workshop. First, Thomas Sterling, Professor of Computer Science at Louisiana State University, gave a keynote talk titled "HPC in Phase Change: Towards a New Parallel Execution Model." Sterling argued that a new multi-dimensional research thrust was required to realize the design goals with regard to power, complexity, clock rate and reliability in the new parallel c- puter systems.ParalleX,anexploratoryexecutionmodeldevelopedbySterling's group was introduced to guide the co-design of new architectures, programming methods and system software.

A Guide to RISC Microprocessors provides a comprehensive coverage of every major RISC microprocessor family. Independent reviewers with extensive technical backgrounds offer a critical perspective in exploring the strengths and weaknesses of all the different microprocessors on the market. This book is organized into seven sections and comprised of 35 chapters. The discussion begins with an overview of RISC architecture intended to help readers understand the technical details and the significance of the new chips, along with instruction set design and design issues for next-generation processors. The chapters that follow focus on the SPARC architecture, SPARC chips developed by Cypress Semiconductor in collaboration with Sun, and Cypress's introduction of redesigned cache and memory management support chips for the SPARC processor. Other chapters focus on Bipolar Integrated Technology's ECL SPARC implementation, embedded SPARC processors by LSI Logic and Fujitsu, the MIPS processor, Motorola 88000 RISC chip set, Intel 860 and 960 microprocessors, and AMD 29000 RISC microprocessor family. This book is a valuable resource for consumers interested in RISC microprocessors.

Intel Xeon Phi Coprocessor Architecture and ToolsThe Guide for Application DevelopersApress

Compilers: Principles and Practice

Android Application Development for the Intel Platform

Programmable Digital Signal Processors

High Performance Parallelism Pearls Volume Two

Intel Xeon Phi Processor High Performance Programming

Progress in Cryptology - INDOCRYPT 2009

Power and Performance: Software Analysis and Optimization is a guide to solving performance problems in modern Linux systems. Power-efficient chips are no help if the software those chips run on is inefficient. Starting with the necessary architectural background as a foundation, the book demonstrates the proper usage of performance analysis tools in order to pinpoint the cause of performance problems, and includes best practices for handling common performance issues those tools identify. Provides expert perspective from a key member of Intel's optimization team on how processors and memory systems influence performance Presents ideas to improve architectures running mobile, desktop, or enterprise platforms Demonstrates best practices for designing experiments and benchmarking throughout the software lifecycle Explains the importance of profiling and measurement to determine the source of performance issues

The number of Android devices running on Intel processors has increased since Intel and Google announced, in late 2011, that they would be working together to optimize future versions of Android for Intel Atom processors. Today, Intel processors can be found in Android smartphones and tablets made by some of the top manufacturers of Android devices, such as Samsung, Lenovo, and Asus. The increase in Android devices featuring Intel processors has created a demand for Android applications optimized for Intel Architecture: Android Application Development for the Intel® Platform is the perfect introduction for software engineers and mobile app developers. Through well-designed app samples, code samples and case studies, the book teaches Android application development based on the Intel platform—including for smartphones, tablets, and embedded devices—covering performance tuning, debugging and optimization. This book is jointly developed for individual learning by Intel Software College and China Shanghai JiaoTong University.

Compilers: Principles and Practice explains the phases and implementation of compilers and interpreters, using a large number of real-life examples. It includes examples from modern software practices such as Linux, GNU Compiler Collection (GCC) and Perl. This book has been class-tested and tuned to the requirements of undergraduate computer engineering courses across universities in India.

This book presents the state of the art in parallel numerical algorithms, applications, architectures, and system software. The book examines various solutions for issues of concurrency, scale, energy efficiency, and programmability, which are discussed in the context of a diverse range of applications. Features: includes contributions from an international selection of world-class authorities; examines parallel algorithm-architecture interaction through issues of computational capacity-based codesign and automatic restructuring of programs using compilation techniques; reviews emerging applications of numerical methods in information retrieval and data mining; discusses the latest issues in dense and sparse matrix computations for modern high-performance systems, multicores, manycores and GPUs, and several perspectives on the Spike family of algorithms for solving linear systems; presents outstanding challenges and developing technologies, and puts these in their historical context.

Languages and Compilers for Parallel Computing

8th Latin American Conference, CARLA 2021, Guadalajara, Mexico, October 6–8, 2021, Revised Selected Papers

Optimized C++

Software Development for Embedded Multi-core Systems

Write Great Code, Vol. 2

Mastering DPC++ for Programming of Heterogeneous Systems using C++ and SYCL

The Cryptographers' Track at the RSA Conference 2018, San Francisco, CA, USA, April 16-20, 2018, Proceedings

Optimizing HPC Applications with Intel® Cluster Tools takes the reader on a tour of the fast-growing area of high performance computing and the optimization of hybrid programs. These programs typically combine distributed memory and shared memory programming models and use the Message Passing Interface (MPI) and OpenMP for multi-threading to achieve the ultimate goal of high performance at low power consumption on enterprise-class workstations and compute clusters. The book focuses on optimization for clusters consisting of the Intel® Xeon processor, but the optimization methodologies also apply to the Intel® Xeon Phi™ coprocessor and heterogeneous clusters mixing both architectures. Besides the tutorial and reference content, the authors address and refute many myths and misconceptions surrounding the topic. The text is augmented and enriched by descriptions of real-life situations.

This book constitutes the refereed post-conference proceedings of the 4th International Workshop on Lightweight Cryptography for Security and Privacy, LightSec 2015, held in Bochum, Germany, in September 2015. The 9 full papers presented were carefully reviewed and selected from 17 submissions. The papers are organized in the following topical sections: cryptanalysis, lightweight constructions, implementation challenges.

This book constitutes the proceedings of the 16th International Workshop on OpenMP, IWOMP 2020, held in Austin, TX, USA, in September 2020. The conference was held virtually due to the COVID-19 pandemic. The 21 full papers presented in this volume were carefully reviewed and selected for inclusion in this book. The papers are organized in topical sections named: performance methodologies; applications; OpenMP extensions; performance studies; tools; NUMA; compilation techniques; heterogeneous computing; and memory. The chapters 'A Case Study on Addressing Complex Load Imbalance in OpenMP' and 'A Study of Memory Anomalies in OpenMP Applications' are available open access under a Creative Commons Attribution 4.0 License via link.springer.com.

*The multicore revolution has reached the deployment stage in embedded systems ranging from small ultramobile devices to large telecommunication servers. The transition from single to multicore processors, motivated by the need to increase performance while conserving power, has placed great responsibility on the shoulders of software engineers. In this new embedded multicore era, the toughest task is the development of code to support more sophisticated systems. This book provides embedded engineers with solid grounding in the skills required to develop software targeting multicore processors. Within the text, the author undertakes an in-depth exploration of performance analysis, and a close-up look at the tools of the trade. Both general multicore design principles and processor-specific optimization techniques are revealed. Detailed coverage of critical issues for multicore employment within embedded systems is provided, including the Threading Development Cycle, with discussions of analysis, design, development, debugging, and performance tuning of threaded applications. Software development techniques engendering optimal mobility and energy efficiency are highlighted through multiple case studies, which provide practical "how-to advice on implementing the latest multicore processors. Finally, future trends are discussed, including terascale, speculative multithreading, transactional memory, interconnects, and the software-specific implications of these looming architectural developments. Table of Contents Chapter 1 - Introduction Chapter 2 – Basic System and Processor Architecture Chapter 3 – Multi-core Processors & Embedded Chapter 4 –Moving To Multi-core Intel Architecture Chapter 5 – Scalar Optimization & Usability Chapter 6 – Parallel Optimization Using Threads Chapter 7 - Case Study: Data Decomposition Chapter 8 - Case Study: Functional Decomposition Chapter 9 – Virtualization & Partitioning Chapter 10 – Getting Ready For Low Power Intel Architecture Chapter 11 - Summary, Trends, and Conclusions Appendix I Glossary References *This is the only book to explain software optimization for embedded multi-core systems *Helpful tips, tricks and design secrets from an Intel programming expert, with detailed examples using the popular X86 architecture *Covers hot topics, including ultramobile devices, low-power designs, Pthreads vs. OpenMP, and heterogeneous cores*

Modeling and Optimization of Parallel and Distributed Embedded Systems

Squeeze the Last Bit of Performance from Your Application.

16th International Workshop on OpenMP, IWOMP 2020, Austin, TX, USA, September 22–24, 2020, Proceedings

Computational Science - ICCS 2006

A Guide to RISC Microprocessors

10th International Conference on Cryptology in India, New Delhi, India, December 13-16, 2009, Proceedings

High-Performance Computing on the Intel® Xeon PhiTM

Om hvordan mikroprocessorer fungerer, med unders ø gelse af de nyeste mikroprocessorer fra Intel, IBM og Motorola.

This book constitutes the refereed proceedings of the Cryptographer's Track at the RSA Conference 2018, CT-RSA 2018, held in San Francisco, CA, USA, in March 2018. The 26 papers presented in this volume were carefully reviewed and selected from 79 submissions. CT-RSA is the track devoted to scientific papers on cryptography, public-key to symmetric-key cryptography and from crypto- graphic protocols to primitives and their implementation security.

It's a critical lesson that today's computer science students aren't always being taught: How to carefully choose their high-level language statements to produce efficient code. Write Great Code, Volume 2: Thinking Low-Level, Writing High-Level shows software engineers what too many college and university courses don't - how compilers translate high-level language statements and data structures into machine code. Armed with this knowledge, they will make informed choices concerning the use of those high-level structures and help the compiler produce far better machine code - all without having to give up the productivity and portability benefits of using a high-level language.

This double volume constitutes the thoroughly refereed post-conference proceedings of the 25th International Conference on Financial Cryptography and Data Security, FC 2021, held online due to COVID-19, in March 2021. The 47 revised full papers and 4 short papers together with 3 as Systematization of Knowledge (SoK) papers were carefully selected and reviewed from 223 submissions. The accepted papers were organized according to their topics in 12 sessions: Smart Contracts, Anonymity and Privacy in Cryptocurrencies, Secure Multi-Party Computation, System and Application Security, Zero-Knowledge Proofs, Blockchain Protocols, Payment Channels, Mining, Scaling Blockchains, Authentication and Usability, Measurement, and Cryptography.

Topics in Cryptology – CT-RSA 2018

Inside the Machine

Software Analysis and Optimization

Knights Landing Edition

Understanding 64-bit Processors and EPIC Principles

6th International Conference, Reading, UK, May 28-31, 2006, Proceedings, Part I

Intel Xeon Phi Coprocessor High Performance Programming

For repairing performance loss or maximizing current potential, this guide aims to provide the information and conceptual framework that will enable readers to be performance experts. Includes information on processor performance, application profiling and hardware considerations.

High Performance Parallelism Pearls Volume 2 offers another set of examples that demonstrate how to leverage parallelism. Similar to Volume 1, the techniques included here explain how to use processors and coprocessors with the same programming – illustrating the most effective ways to combine Xeon Phi coprocessors with Xeon and other multicore processors. The book includes examples of successful programming efforts, drawn from across industries and domains such as biomed, genetics, finance, manufacturing, imaging, and more. Each chapter in this edited work includes detailed explanations of the programming techniques used, while showing high performance results on both Intel Xeon Phi coprocessors and multicore processors. Learn from dozens of new examples and case studies illustrating "success stories" demonstrating not just the features of Xeon-powered systems, but also how to leverage parallelism across these heterogeneous systems. Promotes write-once, run-anywhere coding, showing how to code for high performance on multicore processors and Xeon Phi Examples from multiple vertical domains illustrating real-world use of Xeon Phi coprocessors Source code available for download to facilitate further exploration

This guide provides a comprehensive overview of High Performance Computing (HPC) to equip students with a full skill set including cluster setup, network selection, and a background of supercomputing competitions. It covers the system, architecture, evaluating approaches, and other practical supercomputing techniques. As the world's largest supercomputing hackathon, the ASC Student Supercomputer Challenge has attracted a growing number of new talent to supercomputing and has greatly promoted communications in the global HPC community. Enclosed in this book, readers will also find how to analyze and optimize supercomputing systems and applications in real science and engineering cases.

Java Performance: The Definitive Guide

The Guide for Application Developers

Financial Cryptography and Data Security

14th International Conference, CC 2005, Held as Part of the Joint European Conferences on Theory and Practice of Software, ETAPS 2005

Integrated Circuit and System Design. Power and Timing Modeling, Optimization, and Simulation