Cmos Sram Circuit Design And Parametric Test In Nano Scaled Technologies Process Aware Sram Design And Test Frontiers In Electronic Testing

Market demand for microprocessor performance has motivated continued scaling of CMOS through a succession of lithography generation Quantum mechanical limitations to continued scaling are becoming readily apparent. Partially Depleted Silicon-on-Insulator (PD-SOI) technology is emerging as a promising means of addressing these limitations. It also introduces additional design complexity which must be well understood. SOI Circuit Design Concepts first introduces the student or practicing engineer to SOI device physics and its fundamental idiosyncrasies. It then walks the reader through realizations of these mechanisms which are observed in common high-speed microprocess designs. Rules of thumb and comparisons to conventional bulk CMOS are offered to guide implementation. SOI's ultimate advantage, howe may lie in the unique circuit topologies it supports; a number of these novel new approaches are described as well. SOI Circuit Design Concepts draws upon the latest industry literature as well as the firsthand experiences of its authors. It is an ideal introduction to the concep of governing SOI use and provides a firm foundation for further study of this exciting new technology paradigm.

Take Advantage of Today's Most Sophisticated Techniques for Designing and Simulating Complex CMOS Integrated Circuits! An essential working tool for electronic circuit designers and students alike, Advanced CMOS Cell Design is a practice-based guide to today's most sophisticated design and simulation techniques for CMOS (complementary metal oxide semiconductor) integrated circuits. Written by two internationally renowned circuit designers, this outstanding book presents the state-of-the-art techniques required to design and simulate ev type of CMOS integrated circuit. The reference contains unsurpassed coverage of deep-submicron to nanoscale technologies...SRAM, DRA EEPROM, and Flash...design of a simple microprocessor...configurable logic circuits...data converters... input/output...design rules... and much more. Packed with 100 detailed illustrations, Advanced CMOS Cell Design enables you to: Explore the latest embedded memory architectures Master the programming of logic circuits Get expert guidance on radio frequency (RF) circuit design Learn more about silicon on insulator (SOI) technologies Acquire a full range of circuit simulation tools This Advanced CMOS Circuit Design Toolkit Covers- • Deep-Submicron to Nanoscale Technologies • SRAM, DRAM, EEPROM, and Flash • Design of a Simple Microprocessor • Configurable Logic Circuits • Radio Frequency (RF) Circuit Design • Data Converters • Input/Output • Silicon on Insulator (SOI) Technologies • Impact of Nanotechnologies • Design Rules • Quick-Reference Sheets

This book discusses the digital design of integrated circuits under process variations, with a focus on design-time solutions. The authors describe a step-by-step methodology, going from logic gates to logic paths to the circuit level. Topics are presented in comprehensively, wit overwhelming use of analytical formulations. Emphasis is placed on providing digital designers with understanding of the sources of proces variations, their impact on circuit performance and tools for improving their designs to comply with product specifications. Various circuit-level “design hints” are highlighted, so that readers can use then to improve their designs. A special treatment is devoted to unique design issues and the impact of process variations on the performance of FinFET based circuits. This book enables readers to make optimal decis at design time, toward more efficient circuits, with better yield and higher reliability.

A practical guide to the effects of radiation on semiconductor components of electronic systems, and techniques for the designing, laying ou and testing of hardened integrated circuits This book teaches the fundamentals of radiation environments and their effects on electronic components, as well as how to design, lay out, and test cost-effective hardened semiconductor chips not only for today’s space systems bu commercial terrestrial applications as well. It provides a historical perspective, the fundamental science of radiation, and the basics of semiconductors, as well as radiation-induced failure mechanisms in semiconductor chips. Integrated Circuits Design for Radiation Environments starts by introducing readers to semiconductors and radiation environments (including space, atmospheric, and terrestrial environments) followed by circuit design and layout. The book introduces radiation effects phenomena including single-event effects, total ionizing dose damage and displacement damage) and shows how technological solutions can address both phenomena. Describes the fundamentals of radiation environments and their effects on electronic components Teaches readers how to design, lay out and test cost-effective hardened semiconductor chips for space systems and commercial terrestrial applications Covers natural and man-made radiation environments, space systems and commercial terrestrial applications Provides up-to-date coverage of state-of-the-art of radiation hardenin technology in one concise volume Includes questions and answers for the reader to test their knowledge Integrated Circuits Design for Radiation Environments will appeal to researchers and product developers in the semiconductor, space, and defense industries, as well as electronic engineers in the medical field. The book is also helpful for system, layout, process, device, reliability, applications, ESD, latchup a circuit design semiconductor engineers, along with anyone involved in micro-electronics used in harsh environments.

SOI Circuit Design Concepts

Device Design and Applications

The Design of Low Power CMOS SRAM Subsystems

Circuits and Statistical Design for Yield

Process-Aware Sram Design and Test

Challenges and Applications in the Internet of Things

In this book, Complementary Metal Oxide Semiconductor (CMOS) devices are extensively discussed. The topics encompass the technology advancement in the fabrication process of metal oxide semiconductor field effect transistors or MOSFETs (which are the fundamental building blocks of CMOS devices) and the applications of transistors in the present and future eras. The book is intended to provide information on the latest technology development of CMOS to researchers, physicists, as well as engineers working in the field of semiconductor transistor manufacturing and design.

Variability is one of the most challenging obstacles for IC design in the nanometer regime. In nanometer technologies, SRAM show an increased sensitivity to process variations due to low-voltage operation requirements, which are aggravated by the strong demand for lower power consumption and cost, while achieving higher performance and density. With the drastic increase in memory densities, lower supply voltages, and higher variations, statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power. This book is an invaluable reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design. It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies. Provides comprehensive review of state-of-the-art, variation-tolerant SRAM circuit techniques; Discusses Impact of device related process variations and how they affect circuit and system performance, from a design point of view; Helps designers optimize memory yield, with practical statistical design methodologies and yield estimation techniques.

CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled TechnologiesProcess-Aware SRAM Design and TestSpringer Science & Business Media

During the last decade, CMOS has become increasingly attractive as a basic integrated circuit technology due to its low power (at moderate frequencies), good scalability, and rail-to-rail operation. There are now a variety of CMOS circuit styles, some based on static complementary con ductance properties, but others borrowing from earlier NMOS techniques and the advantages of using clocking disciplines for precharge-evaluate se quencing. In this comprehensive book, the reader is led systematically through the entire range of CMOS circuit design. Starting with the in dividual MOSFET, basic circuit building blocks are described, leading to a broad view of both combinatorial and sequential circuits. Once these circuits are considered in the light of CMOS process technologies, impor tant topics in circuit performance are considered, including characteristics of interconnect, gate delay, device sizing, and I/O buffering. Basic circuits are then composed to form macro elements such as multipliers, where the reader acquires a unified view of architectural performance through par allelism, and circuit performance through careful attention to circuit-level and layout design optimization. Topics in analog circuit design reflect the growing tendency for both analog and digital circuit forms to be combined on the same chip, and a careful treatment of BiCMOS forms introduces the reader to the combination of both FET and bipolar technologies on the same chip to provide improved performance.

Robust SRAM Designs and Analysis

VLSI-SoC: Internet of Things Foundations

Communication, Networks and Computing

Advances in Communications, Signal Processing, and VLSI

Complementary Metal Oxide Semiconductor

Low Power Design Essentials

Low-Power Digital VLSI Design: Circuits and Systems addresses both process technologies and device modeling. Power dissipation in CMOS circuits, several practical circuit examples, and low-power techniques are discussed. Low-voltage issues for digital CMOS and BiCMOS circuits are emphasized. The book also provides an extensive study of advanced CMOS subsystem design. A low-power design methodology is presented with various power minimization techniques at the circuit, logic, architecture and algorithm levels. Features: Low-voltage CMOS device modeling, technology files, design rules Switching activity concept, low-power guidelines to engineering practice Pass-transistor logic families Power dissipation of I/O circuits Multi- and low-VT CMOS logic, static power reduction circuit techniques State of the art design of low-voltage BiCMOS and CMOS circuits Low-power techniques in CMOS SRAMS and DRAMS Low-power on-chip voltage down converter design Numerous advanced CMOS subsystems (e.g. adders, multipliers, data path, memories, regular structures, phase-locked loops) with several design options trading power, delay and area Low-power design methodology, power estimation techniques Power reduction techniques at the logic, architecture and algorithm levels More than 190 circuits explained at the transistor level.

The demand for ever smaller and portable electronic devices has driven metal oxide semiconductor-based (CMOS) technology to its physical limit with the smallest possible feature sizes. This presents various size-related problems such as high power leakage, low-reliability, and thermal effects, and is a limit on further miniaturization. To enable even smaller electronics, various nanodevices including carbon nanotube transistors, graphene transistors, tunnel transistors and memristors (collectively called post-CMOS devices) are emerging that could replace the traditional and ubiquitous silicon transistor. This book explores these nanoelectronics at the device level including modelling and design. Topics covered include high-k dielectrics; high mobility n and p channels on gallium arsenide and silicon substrates using interfacial misfit dislocation arrays; anodic metal-insulator-metal (MIM) capacitors; graphene transistors; junction and doping free transistors; nanoscale gigh-k/metal-gate CMOS and FinFET based logic libraries; multiple-independent-gate nanowire transistors; carbon nanotubes for efficient power delivery; timing driven buffer insertion for carbon nanotube interconnects; memristor modeling; and neuromorphic devices and circuits. This book is essential reading for researchers, research-focused industry designers/developers, and advanced students working on next-generation electronic devices and circuits.

This book comprises the peer-reviewed proceedings of the International Conference on Communications, Signal Processing and VLSI (IC2SV) 2019. It explores the recent advances in the fields of signal and image processing, wireless and mobile communications, embedded systems, VLSI, microwave, and antennas. The contents provide insights into present technological challenges and discusses the emerging applications of different imaging techniques and communications systems. Given the range of topics covered, this book can be useful for students as well as researchers interested in the area of communications, signal processing, and VLSI technologies.

This reference text discusses recent advances in the field of nanotechnology with applications in the fields of electronics sector, agriculture, health services, smart cities, food industry, and energy sector in a comprehensive manner. The text begins by discussing important concepts including bio nanotechnology, nano electronics, nano devices, nano medicine, and nano memories. It then comprehensively covers applications of nanotechnology in different areas including healthcare, energy sector, environment,

security and defense, agriculture sector, food industry, automotive sector, smart cities, and Internet of Things (IoT). Aimed at senior undergraduate, graduate students and professionals in the fields of electrical engineering, electronics engineering, nanoscience and nanotechnology, this text: Discusses nano image sensors useful for imaging in medical and for security applications. Covers advances in the field of nanotechnology with their applications. It covers important concepts including neuro simulators, nano medicine, and nano materials. Covers applications of nanotechnology in diverse fields including health sector, agriculture, energy sector, and electronics.
Digital Design and Fabrication

VLSI Design and Test for Systems Dependability
Advanced CMOS Cell Design
Future Information Technology, Application, and Service
Circuit Design for CMOS VLSI

This book contains all the topics of importance to the low power designer. It first lays the foundation and then goes on to detail the design process. The book also discusses such special topics as power management and modal design, ultra low power, and low power design methodology and flows. In addition, coverage includes projections of the future and case studies.

This is an up-to-date treatment of the analysis and design of CMOS integrated digital logic circuits. The self-contained book covers all of the important digital circuit design styles found in modern CMOS chips, emphasizing solving design problems using the various logic styles available in CMOS.

The monograph will be dedicated to SRAM (memory) design and test issues in nano-scaled technologies by adapting the cell design and chip design considerations to the growing process variations with associated test issues. Purpose: provide process-aware solutions for SRAM design and test challenges.

This book is proceedings of the 7th FTRA International Conference on Future Information Technology (FutureTech 2012). The topics of FutureTech 2012 cover the current hot topics satisfying the world-wide ever-changing needs. The FutureTech 2012 is intended to foster the dissemination of state-of-the-art research in all future IT areas, including their models, services, and novel applications associated with their utilization. The FutureTech 2012 will provide an opportunity for academic and industry professionals to discuss the latest issues and progress in this area. In addition, the conference will publish high quality papers which are closely related to the various theories, modeling, and practical applications in many types of future technology. The main scope of FutureTech 2012 is as follows. Hybrid Information Technology Cloud and Cluster Computing Ubiquitous Networks and Wireless Communications Multimedia Convergence Intelligent and Pervasive Applications Security and Trust Computing IT Management and Service Bioinformatics and Bio-Inspired Computing Database and Data Mining Knowledge System and Intelligent Agent Human-centric Computing and Social Networks The FutureTech is a major forum for scientists, engineers, and practitioners throughout the world to present the latest research, results, ideas, developments and applications in all areas of future technologies.

Low-power, Low-voltage SRAM Circuits Design for Nanometric CMOS Technologies
Advances in Signal Processing and Communication
CMOS Memory Circuits
CMOS SRAM Design and Analysis of Low Leakage and High Speed SRAM Cell
Integrated Circuit Design for Radiation Environments
22nd IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2014, Playa del Carmen, Mexico, October 6-8, 2014, Revised Selected Papers

Nanotechnology ("nanotech") is the manipulation of matter on an atomic, molecular, and supramolecular scale. The earliest, widespread description of nanotechnology referred to the particular technological goal of precisely manipulating atoms and molecules for fabrication of macroscale products, also now referred to as molecular nanotechnology. A more generalized description of nanotechnology was subsequently established by the National Nanotechnology Initiative, which defines nanotechnology as the manipulation of matter with at least one dimension sized from 1 to 100 nanometers. This definition reflects the fact that quantum mechanical effects are important at this quantum-realm scale, and so the definition shifted from a particular technological goal to a research category inclusive of all types of research and technologies that deal with the special properties of matter that occur below the given size threshold. It is therefore common to see the plural form "nanotechnologies" as well as "nanoscale technologies" to refer to the broad range of research and applications whose common trait is size. Because of the variety of potential applications (including industrial and military), governments have invested billions of dollars in nanotechnology research. Through its National Nanotechnology Initiative, the USA has invested 3.7 billion dollars. The European Union has invested[when?] 1.2 billion and Japan 750 million dollars.

FPGA Architecture: Survey and Challenges reviews the historical development of programmable logic devices, the fundamental programming technologies that the programmability is built on, and then describes the basic understandings gleaned from research on architectures. It is an invaluable reference for engineers and computer scientists. It is also an excellent primer for senior or graduate-level students in electrical engineering or computer science.

This book provides a comprehensive overview of contemporary issues in complementary metal-oxide semiconductor (CMOS) device design, describing how to overcome process-induced random variations such as line-edge-roughness, random-dopant-fluctuation, and work-function variation, and the applications of novel CMOS devices to cache memory (or Static Random Access Memory, SRAM). The author places emphasis on the physical understanding of process-induced random variation as well as the introduction of novel CMOS device structures and their application to SRAM. The book outlines the technical predicament facing state-of-the-art CMOS technology development, due to the effect of ever-increasing process-induced random/intrinsic variation

in transistor performance at the sub-30-nm technology nodes. Therefore, the physical understanding of process-induced random/intrinsic variations and the technical solutions to address these issues plays a key role in new CMOS technology development. This book aims to provide the reader with a deep understanding of the major random variation sources, and the characterization of each random variation source. Furthermore, the book presents various CMOS device designs to surmount the random variation in future CMOS technology, emphasizing the applications to SRAM.

BiCMOS Technology and Applications, Second Edition provides a synthesis of available knowledge about the combination of bipolar and MOS transistors in a common integrated circuit - BiCMOS. In this new edition all chapters have been updated and completely new chapters on emerging topics have been added. In addition, BiCMOS Technology and Applications, Second Edition provides the reader with a knowledge of either CMOS or Bipolar technology/design a reference with which they can make educated decisions regarding the viability of BiCMOS in their own application. BiCMOS Technology and Applications, Second Edition is vital reading for practicing integrated circuit engineers as well as technical managers trying to evaluate business issues related to BiCMOS. As a textbook, this book is also appropriate at the graduate level for a special topics course in BiCMOS. A general knowledge in device physics, processing and circuit design is assumed. Given the division of the book, it lends itself well to a two-part course; one on technology and one on design. This will provide advanced students with a good understanding of tradeoffs between bipolar and MOS devices and circuits.

ISTFA 2018: Proceedings from the 44th International Symposium for Testing and Failure Analysis

Select Proceedings of ICSC 2018

Proceedings of Second International Conference on Smart Energy and Communication

CMOS Logic Circuit Design

Circuit Design, Layout, and Simulation

Survey and Challenges

This book discusses the new roles that the VLSI (very-large-scale integration of semiconductor circuits) is taking for the safe, secure, and dependable design and operation of electronic systems. The book consists of three parts. Part I, as a general introduction to this vital topic, describes how electronic systems are designed and tested with particular emphasis on dependability engineering, where the simultaneous assessment of the detrimental outcome of failures and cost of their containment is made. This section also describes the related research project “Dependable VLSI Systems,” in which the editor and authors of the book were involved for 8 years. Part II addresses various threats to the dependability of VLSIs as key systems components, including time-dependent degradations, variations in device characteristics, ionizing radiation, electromagnetic interference, design errors, and tampering, with discussion of technologies to counter those threats. Part III elaborates on the design and test technologies for dependability in such applications as control of robots and vehicles, data processing, and storage in a cloud environment and heterogeneous wireless telecommunications. This book is intended to be used as a reference for engineers who work on the design and testing of VLSI systems with particular attention to dependability. It can be used as a textbook in graduate courses as well. Readers interested in dependable systems from social and industrial–economic perspectives will also benefit from the discussions in this book.

The International Symposium for Testing and Failure Analysis (ISTFA) 2018 is co-located with the International Test Conference (ITC) 2018, October 28 to November 1, in Phoenix, Arizona, USA at the Phoenix Convention Center. The theme for the November 2018 conference is "Failures Worth Analyzing." While technology advances fast and the market demands the latest and the greatest, successful companies strive to stay competitive and remain profitable.

In response to tremendous growth and new technologies in the semiconductor industry, this volume is organized into five, information-rich sections. Digital Design and Fabrication surveys the latest advances in computer architecture and design as well as the technologies used to manufacture and test them. Featuring contributions from leading experts, the book also includes a new section on memory and storage in addition to a new chapter on nonvolatile memory technologies. Developing advanced concepts, this sharply focused book— Describes new technologies that have become driving factors for the electronic industry Includes new information on semiconductor memory circuits, whose development best illustrates the phenomenal progress encountered by the fabrication and technology sector Contains a section dedicated to issues related to system power consumption Describes reliability and testability of computer systems Pinpoints trends and state-of-the-art advances in fabrication and CMOS technologies Describes performance evaluation measures, which are the bottom line from the user’s point of view Discusses design techniques used to create modern computer systems, including high-speed computer arithmetic and high-frequency design, timing and clocking, and PLL and DLL design

This book comprises select proceedings of the International Conference on VLSI, Communication and Signal processing (VCAS 2018). It looks at latest research findings in VLSI design and applications. The book covers a wide range of topics in electronics and communication engineering, especially in the area of microelectronics and VLSI design, communication systems and networks, and image and signal processing. The contents of this book will be useful to researchers and professionals alike.

Low-Power Digital VLSI Design

Proceedings of ICMEET 2017

CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies

Emerging Trends in Photonics, Signal Processing and Communication Engineering

BiCMOS Technology and Applications

Microelectronics, Electromagnetics and Telecommunications

This book (CCIS 839) constitutes the refereed proceedings of the First International Conference on Communication, Networks and Computings, CNC 2018, held in Gwalior, India, in March 2018. The 70 full papers were carefully reviewed and selected from 182 submissions. The papers are organized in topical sections on wired and wireless communication systems, high dimensional data representation and processing, networks and information security, computing techniques for efficient networks design, electronic circuits for communication system.

Success in the development of recent advanced semiconductor device technologies is due to the success of SRAM memory cells. This book addresses various issues for designing SRAM memory cells for advanced CMOS technology. To study LSI design, SRAM cell design is the best materials subject because issues about variability, leakage and reliability have to be taken into account for the design.

Praise for CMOS: Circuit Design, Layout, and SimulationRevised Second Edition from the Technical Reviewers "A refreshing industrial flavor. Design

concepts are presented as they are needed for 'just-in-time' learning. Simulating and designing circuits using SPICE is emphasized with literally hundreds of examples. Very few textbooks contain as much detail as this one. Highly recommended!" --Paul M. Furth, New Mexico State University "This book builds a solid knowledge of CMOS circuit design from the ground up. With coverage of process integration, layout, analog and digital models, noise mechanisms, memory circuits, references, amplifiers, PLLs/DLLs, dynamic circuits, and data converters, the text is an excellent reference for both experienced and novice designers alike." --Tyler J. Gomm, Design Engineer, Micron Technology, Inc. "The Second Edition builds upon the success of the first with new chapters that cover additional material such as oversampled converters and non-volatile memories. This is becoming the de facto standard textbook to have on every analog and mixed-signal designer's bookshelf." --Joe Walsh, Design Engineer, AMI Semiconductor CMOS circuits from design to implementation CMOS: Circuit Design, Layout, and Simulation, Revised Second Edition covers the practical design of both analog and digital integrated circuits, offering a vital, contemporary view of a wide range of analog/digital circuit blocks, the BSIM model, data converter architectures, and much more. This edition takes a two-path approach to the topics: design techniques are developed for both long- and short-channel CMOS technologies and then compared. The results are multidimensional explanations that allow readers to gain deep insight into the design process. Features include: Updated materials to reflect CMOS technology's movement into nanometer sizes Discussions on phase- and delay-locked loops, mixed-signal circuits, data converters, and circuit noise More than 1,000 figures, 200 examples, and over 500 end-of-chapter problems In-depth coverage of both analog and digital circuit-level design techniques Real-world process parameters and design rules The book's Web site, CMOSedu.com, provides: solutions to the book's problems; additional homework problems without solutions; SPICE simulation examples using HSPICE, LTspice, and WinSpice; layout tools and examples for actually fabricating a chip; and videos to aid learning

This book contains extended and revised versions of the best papers presented at the 22nd IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2014, held in Playa del Carmen, Mexico, in October 2014. The 12 papers included in the book were carefully reviewed and selected from the 33 full papers presented at the conference. The papers cover a wide range of topics in VLSI technology and advanced research. They address the current trend toward increasing chip integration and technology process advancements bringing about stimulating new challenges both at the physical and system-design levels, as well as in the test of these systems.

Low Power and Reliable SRAM Memory Cell and Array Design

Advances in VLSI, Communication, and Signal Processing

Electronic Devices and Circuit Design

Devices and Modelling

Select Proceedings of VCAS 2018

Nano-cmos and Post-cmos Electronics

This book presents a collection of peer-reviewed articles from the 7th International Conference on Microelectronics, Circuits, and Systems – Micro 2020. The volume covers the latest development and emerging research topics of material sciences, devices, microelectronics, circuits, nanotechnology, system design and testing, simulation, sensors, photovoltaics, optoelectronics, and its different applications. This book also deals with several tools and techniques to match the theme of the conference. It will be a valuable resource for researchers, professionals, Ph.D. scholars, undergraduate and postgraduate students working in Electronics, Microelectronics, Electrical, and Computer Engineering.

The low power circuit design technique has been the trend in developing portable and smaller size electronic products, especially for communication peripherals. In the limitation on the device technology, intergrated design work has played an important role in performing various low power techniqes. This thesis presents the design of low power Complementary Metal Oxide Semiconductor (CMOS) Static Random Access Memory (SRAM) Subsystems. CMOS technology performs much lower static power dissipation compares to other technologies. The implementation of this design by using 3.3 V supply voltage has effectively reduced the dynamic power dissipation of the circuitry. Low power is achieved by implemting 6T-memory cell. Low power techniques are also achieved on capacitance reduction by using divided word-line structure for address decoder. Finally lowe power is achieved by the operating voltage reduction using current-mode sensing technique for sense amplifier with the pre-charge of Vdd/ 2.

Embedded SRAM memory is a vital component in modern SoCs. More than 80% of the System-on-Chip (SoC) die area is often occupied by SRAM arrays. As such, system reliability and yield is largely governed by the SRAM's performance and robustness. The aggressive scaling trend in CMOS device minimum feature size, coupled with the growing demand in high-capacity memory integration, has imposed the use of minimal size devices to realize a memory bitcell. The smallest 6T SRAM bitcell to date occupies a 0.1um2 in silicon area. SRAM bitcells continue to benefit from an aggressive scaling trend in CMOS technologies. Unfortunately, other system components, such as interconnects, experience a slower scaling trend. This has resulted in dramatic deterioration in a cell's ability to drive a heavily-loaded interconnects. Moreover, the growing fluctuation in device properties due to Process, Voltage, and Temperature (PVT) variations has added more uncertainty to SRAM operation. Thus ensuring the ability of a miniaturized cell to drive heavily-loaded bitlines and to generate adequate voltage swing is becoming challenging. A large percentage of state-of-the-art SoC system failures are attributed to the inability of SRAM cells to generate the targeted bitline voltage swing within a given access time. The use of read-assist mechanisms and current mode sense amplifiers are the two key strategies used to surmount bitline loading effects. On the other hand, new bitcell topologies and cell supply voltage management are used to overcome fluctuations in device properties. In this research we tackled conventional 6T SRAM bitcell limited drivability by introducing new integrated voltage sensing schemes and current-mode sense amplifiers. The proposed schemes feature a read-assist mechanism. The proposed schemes' functionality and superiority over existing schemes are verified using transient and statistical SPICE simulations. Post-layout extracted views of the devices are used for realistic simulation results. Low-voltage operated SRAM reliability and yield enhancement is investigated and a wordline boost technique is proposed as a means to manage the cell's WL operating voltage. The proposed wordline driver design shows a significant improvement in reliability and yield in a 400-mV 6T SRAM cell. The proposed wordline driver design exploit the cell's Dynamic Noise Margin (DNM), therefore boost peak level and boost decay rate programmability features are added. SPICE transient and statistical simulations are used to verify the proposed design's functionality. Finally, at a bitcell-level, we proposed a new five-transistor (5T) SRAM bitcell which shows competitive performance and reliability figures of merit compared to the conventional 6T bitcell. The functionality of the proposed cell is verified by post-layout SPICE simulations. The proposed bitcell topology is designed, implemented and fabricated in a standard ST CMOS 65nm technology process. A 1.2_ 1.2 mm2 multi-design project test chip consisting of four 32-Kbit (256-row x 128-column) SRAM macros with the required peripheral and timing control units is fabricated. Two of the designed SRAM macros are dedicated for this work, namely, a 32-Kbit 5T macro and a 32-Kbit 6T macro which is used as a comparison reference. Other macros belong to other projects and are not discussed in this document.

This book gathers selected papers presented at the 2nd International Conference on Smart Energy and Communication (ICSEC 2020), held at Poornima Institute of Engineering and Technology, Jaipur, India, on March 20–21, 2020. It covers a range of topics in electronics and communication engineering and electrical engineering, including analog circuit design, image processing, wireless and microwave communication, optoelectronics and photonic devices, nano-electronics, renewable energy, smart grid, power systems and industry applications.

Nanotechnology

Timing Performance of Nanometer Digital Circuits Under Process Variations

CMOS

Select Proceedings of 7th International Conference on Micro2020

ICSEC 2020

FutureTech 2012 Volume 1

This new volume offers a broad view of the challenges of electronic devices and circuits for IoT applications. The book presents the basic concepts and fundamentals behind new low power, high-speed efficient devices, circuits, and systems in addition to CMOS. It provides an understanding of new materials to improve device performance with smaller dimensions and lower costs. It also looks at the new methodologies to enhance system performance and provides key parameters for exploring the devices and circuit performance based on smart applications. The chapters delve into myriad aspects of circuit design, including MOSFET structures depending on their low power applications for IoT-enabled systems, advanced sensor design and fabrication using MEMS, indirect bootstrap techniques, efficient CMOS comparators, various encryption-decryption algorithms, IoT video forensics applications, microstrip patch antennas in embedded IoT applications, real-time object detection using sound, IOT and nanotechnologies based wireless sensors, and much more.

The volume contains 94 best selected research papers presented at the Third International Conference on Micro Electronics, Electromagnetics and Telecommunications (ICMEET 2017) The conference was held during 09-10, September, 2017 at Department of Electronics and Communication Engineering, BVRIT Hyderabad College of Engineering for Women, Hyderabad, Telangana, India. The volume includes original and application based research papers on microelectronics, electromagnetics, telecommunications, wireless communications, signal/speech/video processing and embedded systems.

This book is a collection of selected peer-reviewed papers presented at the International Conference on Signal Processing and Communication (ICSC 2018). It covers current research and developments in the fields of communications, signal processing, VLSI circuits and systems, and embedded systems. The book offers in-depth discussions and analyses of latest problems across different sub-fields of signal processing and communications. The contents of this book will prove to be useful for students, researchers, and professionals working in electronics and electrical engineering, as well as other allied fields.

CMOS Memory Circuits is a systematic and comprehensive reference work designed to aid in the understanding of CMOS memory circuits, architectures, and design techniques. CMOS technology is the dominant fabrication method and almost the exclusive choice for semiconductor memory designers. Both the quantity and the variety of complementary-metal-oxide-semiconductor (CMOS) memories are staggering. CMOS memories are traded as mass-products worldwide and are diversified to satisfy nearly all practical requirements in operational speed, power, size, and environmental tolerance. Without the outstanding speed, power, and packing density characteristics of CMOS memories, neither personal computing, nor space exploration, nor superior defense systems, nor many other feats of human ingenuity could be accomplished. Electronic systems need continuous improvements in speed performance, power consumption, packing density, size, weight, and costs. These needs continue to spur the rapid advancement of CMOS memory processing and circuit technologies. CMOS Memory Circuits is essential for those who intend to (1) understand, (2) apply, (3) design and (4) develop CMOS memories.

Select Proceedings of IC2SV 2019

Microelectronics, Circuits and Systems

First International Conference, CNC 2018, Gwalior, India, March 22-24, 2018, Revised Selected Papers

Nanometer Variation-Tolerant SRAM

CMOS Sram Circuit Design and Parametric Test in Nano-Scaled Technologies

Process-Aware SRAM Design and Test

This book first introduces SOI device physics and its fundamental idiosyncrasies. It then walks the reader through realizations of these mechanisms, which are observed in common high-speed microprocessor designs. The book also offers rules of thumb and comparisons to conventional bulk CMOS to guide implementation and describes a number of unique circuit topologies that SOI supports.

This volumes presents select papers presented during the International Conference on Photonics, Communication and Signal Processing Technologies held in Bangalore from July 18th to 20th, 2018. The research papers highlight analytical formulation, solution, simulation, algorithm development, experimental research, and experimental investigations in the broad domains of photonics, signal processing and communication technologies. This volume will be of interest to researchers working in the field.

This book provides a guide to Static Random Access Memory (SRAM) bitcell design and analysis to meet

the nano-regime challenges for CMOS devices and emerging devices, such as Tunnel FETs. Since process variability is an ongoing challenge in large memory arrays, this book highlights the most popular SRAM bitcell topologies (benchmark circuits) that mitigate variability, along with exhaustive analysis. Experimental simulation setups are also included, which cover nano-regime challenges such as process variation, leakage and NBTI for SRAM design and analysis. Emphasis is placed throughout the book on the various trade-offs for achieving a best SRAM bitcell design. Provides a complete and concise introduction to SRAM bitcell design and analysis; Offers techniques to face nano-regime challenges such as process variation, leakage and NBTI for SRAM design and analysis; Includes simulation set-ups for extracting different design metrics for CMOS technology and emerging devices; Emphasizes different trade-offs for achieving the best possible SRAM bitcell design.

Proceedings of ICPSPCT 2018

Variation-Aware Advanced CMOS Devices and SRAM

FPGA Architecture

Circuits and Systems